VMIVME-DMA

VMEbus DMA INTERFACE

INSTRUCTION MANUAL

SECOND EDITION

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VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308
(205) 880-0444
1-800-322-3616

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RECORD OF REVISIONS

REVISION LETTER	DATE	PAGES INVOLVED	CHANGE NUMBER
A	05/24/88	Release Manual	88-0090
B	06/06/88	Section 4, Section 5	88-0119
C	07/11/88	Table of Contents, Appendix A	88-0137
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SAFETY SUMMARY

THE FOLLOWING GENERAL SAFETY PRECAUTIONS MUST BE OBSERVED DURING ALL PHASES OF THIS OPERATION, SERVICE, AND REPAIR OF THIS PRODUCT. FAILURE TO COMPLY WITH THESE PRECAUTIONS OR WITH SPECIFIC WARNINGS ELSEWHERE IN THIS MANUAL VIOLATES SAFETY STANDARDS OF DESIGN, MANUFACTURE, AND INTENDED USE OF THE PRODUCT. VME MICROSYSTEMS INTERNATIONAL CORPORATION ASSUMES NO LIABILITY FOR THE CUSTOMER'S FAILURE TO COMPLY WITH THESE REQUIREMENTS.

GROUND THE SYSTEM

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY SYSTEM

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VME Microsystems International Corporation for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS SYSTEM. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.

SAFETY SYMBOLS

GENERAL DEFINITIONS OF SAFETY SYMBOLS USED IN THIS MANUAL

Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the system.

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).

OR

Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.

OR

Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).

Direct current (power line).

Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE: The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

VMIVME-DMA
VMEbus DMA Interface

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SECTION 1

INTRODUCTION

1.1 INTRODUCTION

The VMIVME-DMA VMEbus DMA Interface is a general-purpose DMA interface that is compatible with the VMEbus. It can be interfaced with a user's device or connected back-to-back with another VMIVME-DMA to form a high performance VMEbus-to-VMEbus link. Features of the VMIVME-DMA include the following:

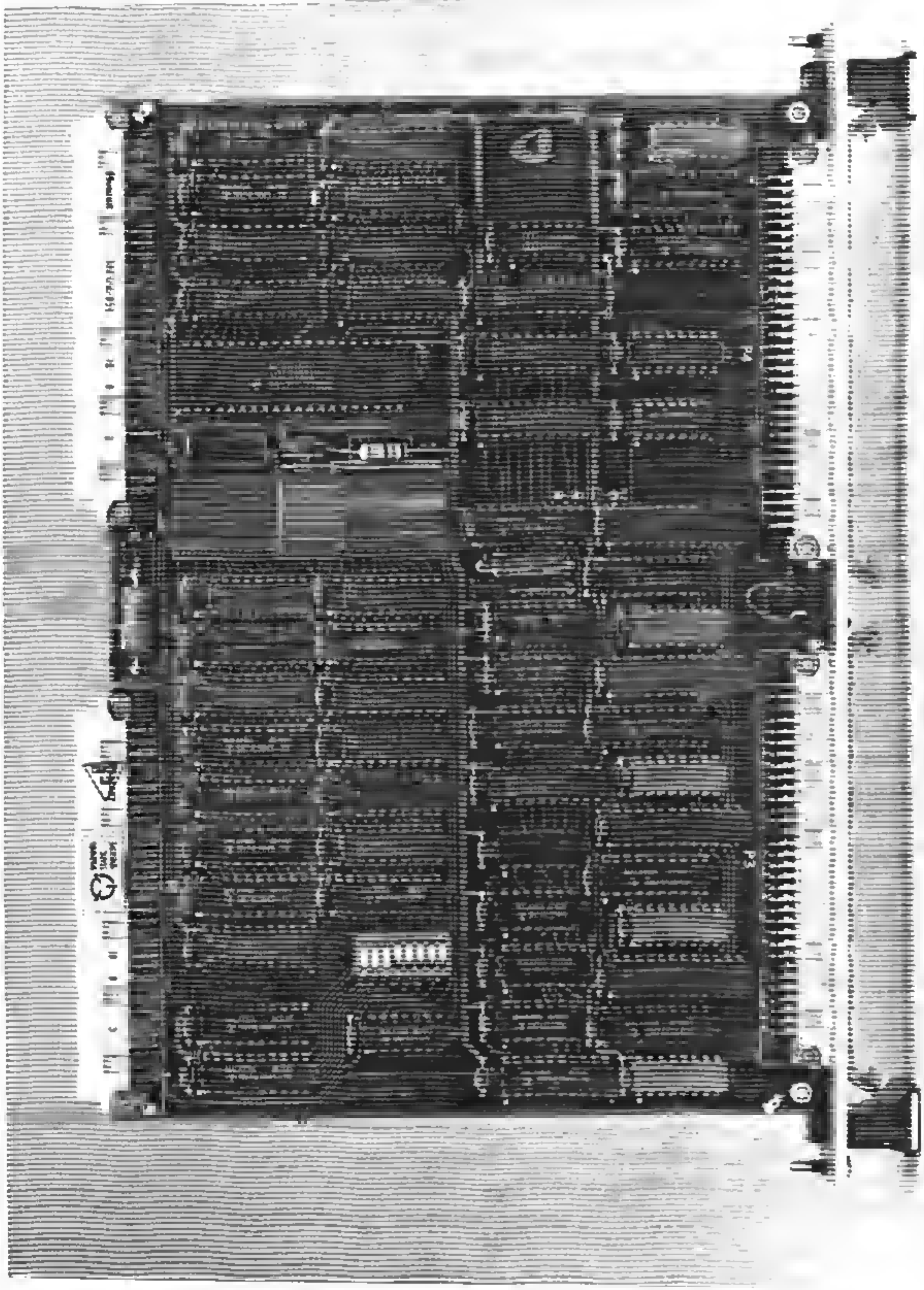
a. 8-, 16-, and 32-bit parallel DMA data transfers
b. Simple handshake
c. VMEbus-to-VMEbus link using two VMIVME-DMAs
d. Programmable address modifiers
e. Interrupt for user's device
f. Programmable interrupt vectors and levels
g. Burst or single-cycle transfers
h. Switch selectable module address

1.2 FUNCTIONAL DESCRIPTION

The VMIVME-DMA provides a general purpose DMA interface that allows a user's device to be connected to the VMEbus. The VMIVME-DMA Board (see Figure 1.2-1) incorporates a 68430 DMA integrated circuit to control DMA transfer by providing the logic necessary to control the VMEbus during transfers and to control the handshake with the user's device. A typical configuration is shown in Figure 1.2-2. The VMIVME-DMA also has the capability of operating in a back-to-back configuration with another VMIVME-DMA to provide a VMEbus-to-VMEbus link (see Figure 1.2-3). If both VMEbuses implement a 32-bit data path, the 32-bit transfers can be performed.

The VMIVME-DMA provides a simple request/acknowledge and *data ready/data taken* handshake to the user's device. For more detailed information, see Section 3, Theory of Operation. The 68430 used in the VMIVME-DMA is software compatible with the 68440 and the 68450, and it also has the capability of performing 32-bit transfers in a single cycle.

The VMIVME-DMA provides a user programmable on-board interrupter. This allows the user's device to generate a VMEbus interrupt. This interrupt may be enabled or disabled by the user, and provides a software programmable vector.



MDMA/F1.2-1

Figure 1.2-1. VMIVME-DMA Photograph

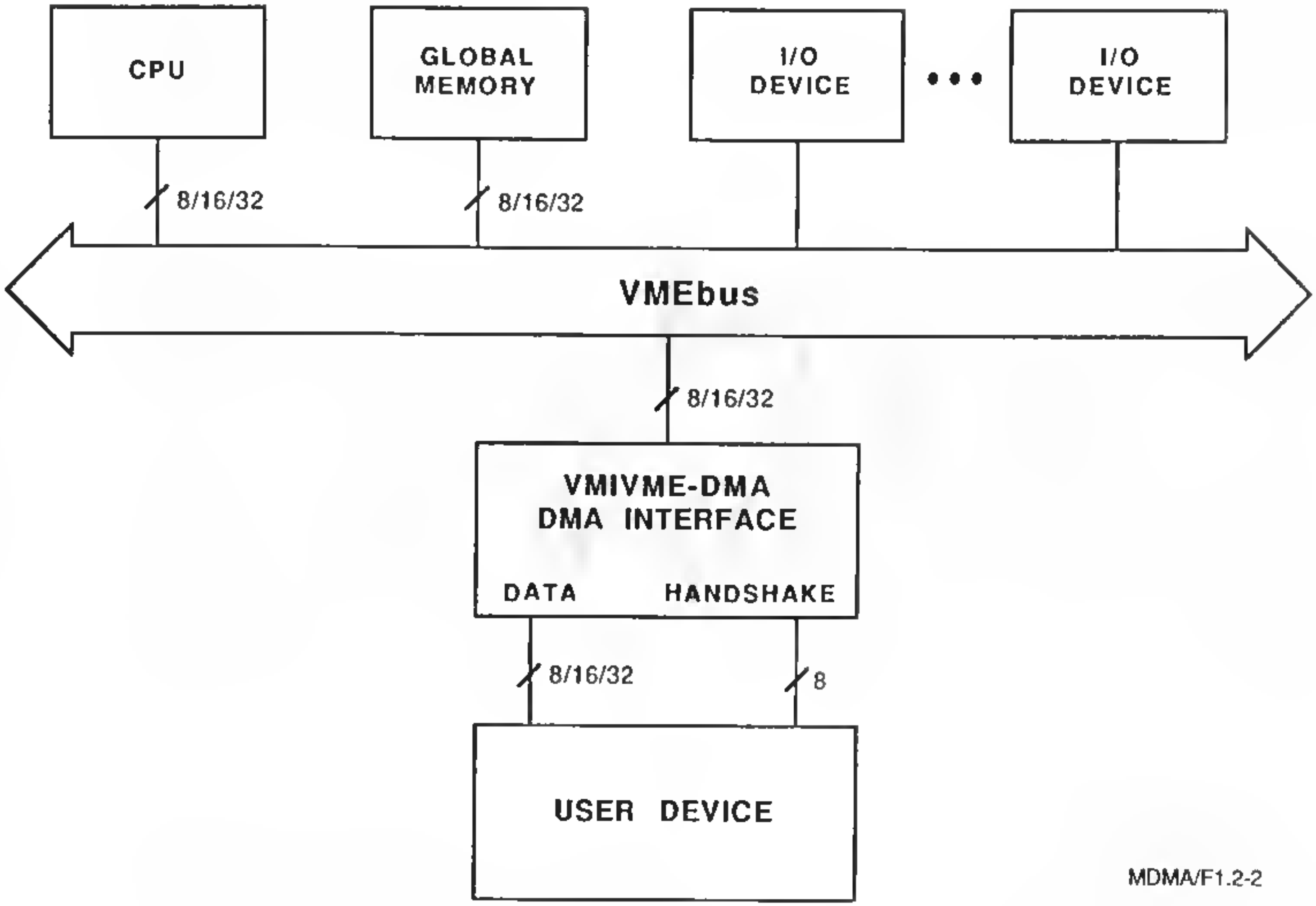


Figure 1.2-2. Typical VMIVME-DMA Configuration with User Device

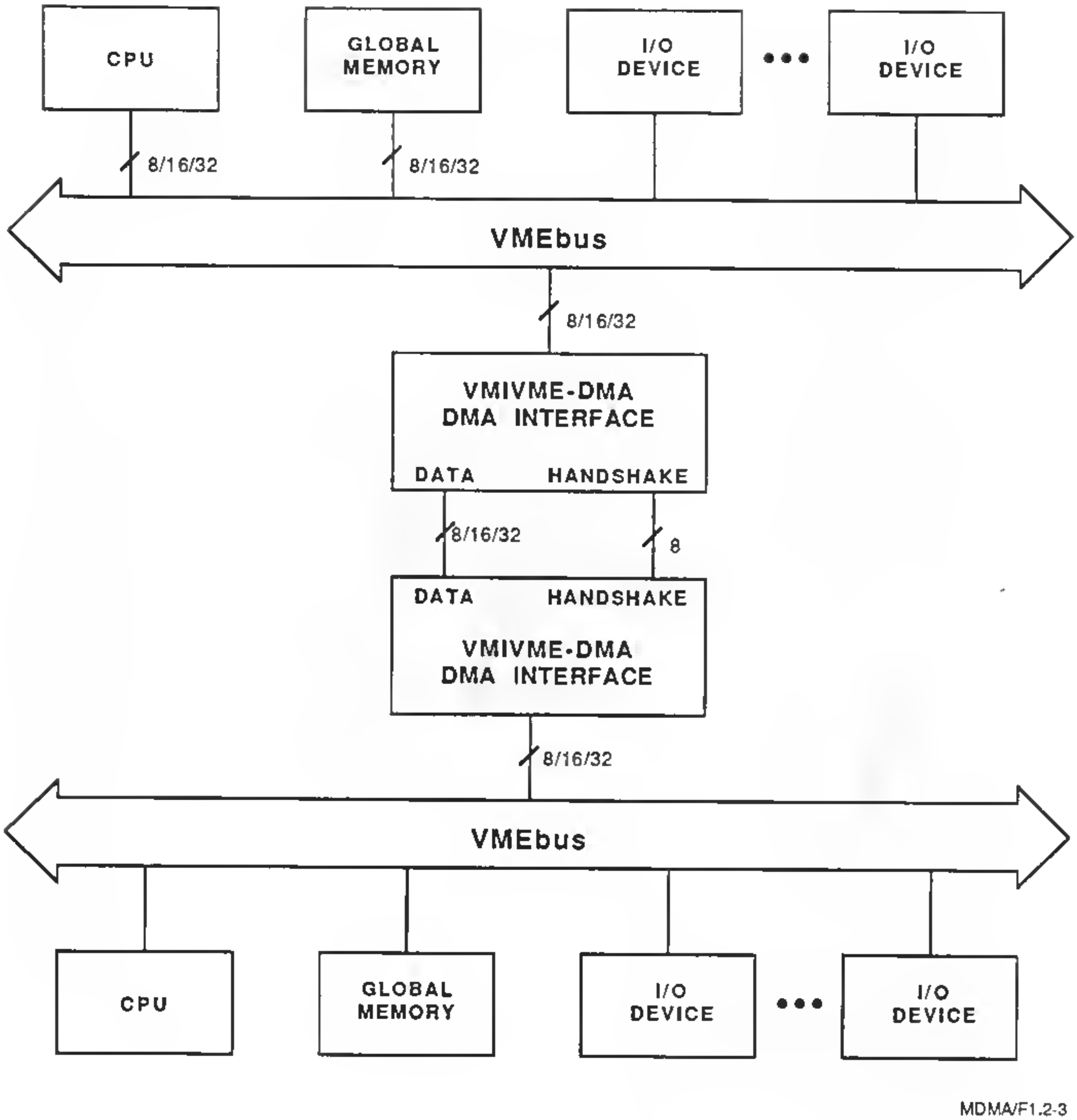


Figure 1.2-3. Typical VMIVME-DMA Back-to-Back Configuration

The VMIVME-DMA also provides a user-programmable output that may be used to interrupt and alert the user's device.

1.3 REFERENCE MATERIAL LIST

The reader should refer to "The VMEbus Specification" for a detailed explanation of VMEbus. "The VMEbus Specification" is available from the following source:

VITA
VMEbus International Trade Association
10229 N. Scottsdale Road
Scottsdale, AZ 85253
(602) 951-8866

SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

2.1 PHYSICAL DESCRIPTION

The VMIVME-DMA interface is implemented on a double Eurocard form factor printed circuit board. Connection to a user's device, or to another VMIVME-DMA, is accomplished via two 64-conductor flat-ribbon cables accessible from the front panel. The VMIVME-DMA has two male DIN connectors (Panduit No. 100-964-053) which mate with DIN connectors designed for flat-ribbon cables (Panduit No. 120-964-455).

2.2 DETAILED SPECIFICATIONS

Detailed specifications are shown in Section 2.3. Transfer rates listed are a function of the speed of global memories and interconnecting cable length. Specifications listed were measured using two DMA boards connected back-to-back as a VMEbus communication link.

The user should refer to Section 5 of this manual for additional information concerning the configuration and installation of this product.

2.3 SPECIFICATIONS

<u>VMEbus MASTER/SLAVE</u>

As a master:	A16:A24:D8:D16:D32 Bus request levels 0, 1, 2, or 3 (jumper selectable)
As a slave:	A16:D8:D16 Addressable on 256-byte boundaries

<u>TRANSFER SPECIFICATIONS</u>

Maximum Transfer Rate	
Burst:	4.65 Megabytes/sec (0.86 µs/transfer)*
Single Cycle:	2.3 Megabytes/sec (1.74 µs/transfer)*
Transfer Mode:	Bidirectional half duplex

*Transfer rates degrade as function of cable length and memory access time. Rates specified are for 125 ns memory and 25-foot cables. Add 4 nanoseconds per foot per transfer.

Transfer Size:	8, 16, 32 bits**
Maximum Block Size:	256 K-4 bytes
Word Counter Range:	16 bits
Address Counter Range:	24 bits

<u>I/O CABLES (not included)</u>

Connection Cables:	Two 64-conductor flat-ribbon cables
Maximum Cable Length:*	50 feet

<u>POWER REQUIREMENTS</u>	3.0 A typical at +5 VDC

<u>ENVIRONMENTAL REQUIREMENTS</u>

Temperature Range:	0° to 55 °C, Operating -20° to 85 °C, Storage
Relative Humidity Range:	20% to 80%, non-condensing

<u>PHYSICAL DIMENSIONS</u>

Double Eurocard 160 mm x 233.4 mm x 12 mm EXP

*Transfer rates degrade as function of cable length and memory access time. Rates specified are for 125 ns memory and 25-foot cables. Add 4 nanoseconds per foot per transfer.

**32-bit global memory required.

SECTION 3

THEORY OF OPERATION

3.1 BLOCK DIAGRAMS

As shown in the functional block diagram (see Figure 3.1-1), the VMIVME-DMA interface provides for the exchange of program controlled interrupts and status, as well as a 32-bit data bus with handshake signals. The functions of these interface signals are described in Section 3.9. The handshake sequencing of the signals is depicted in Figures 3.1-2 and 3.1-3. Although the VMIVME-DMA interface was developed for high-speed, 32-bit, VMEbus link communications, it may also be used as a general purpose DMA controller.

3.2 OPERATIONAL OVERVIEW

The VMIVME-DMA may be utilized in a VME-to-VME link (back-to-back configuration) or linked to an external device. In a VME-to-VME link, the VMIVME-DMA communicates with another DMA board in a separate VMEbus chassis. The VMIVME-DMA may communicate with a user's device provided, however, that custom logic is added to a compatibility board.

To operate in any application, a transfer protocol (see Section 3.3) must be established. Once this is determined, the VMIVME-DMA may be programmed, as detailed in Section 4.1. The operation of this device requires that the bus transfer type (word/byte and direction) is set before the start of any data transfers, and not on a cycle-by-cycle basis. Detailed functional block diagrams of all major logic sections of the DMA board are shown in the figures throughout this section of the manual.

3.3 TRANSFER PROTOCOL

In order for DMA transfers to take place, the DMA interfaces must be set up at both ends of the link. Therefore, if a CPU on one bus is to set up a data transfer, a second CPU on the second bus must set up the DMA interface on that bus to the correct memory address, word count, and direction of transfer.

The manner in which CPUs in two separate buses determine the proper setup sequences is referred to as the transfer protocol. There are several types of protocols that may be used with the DMA.

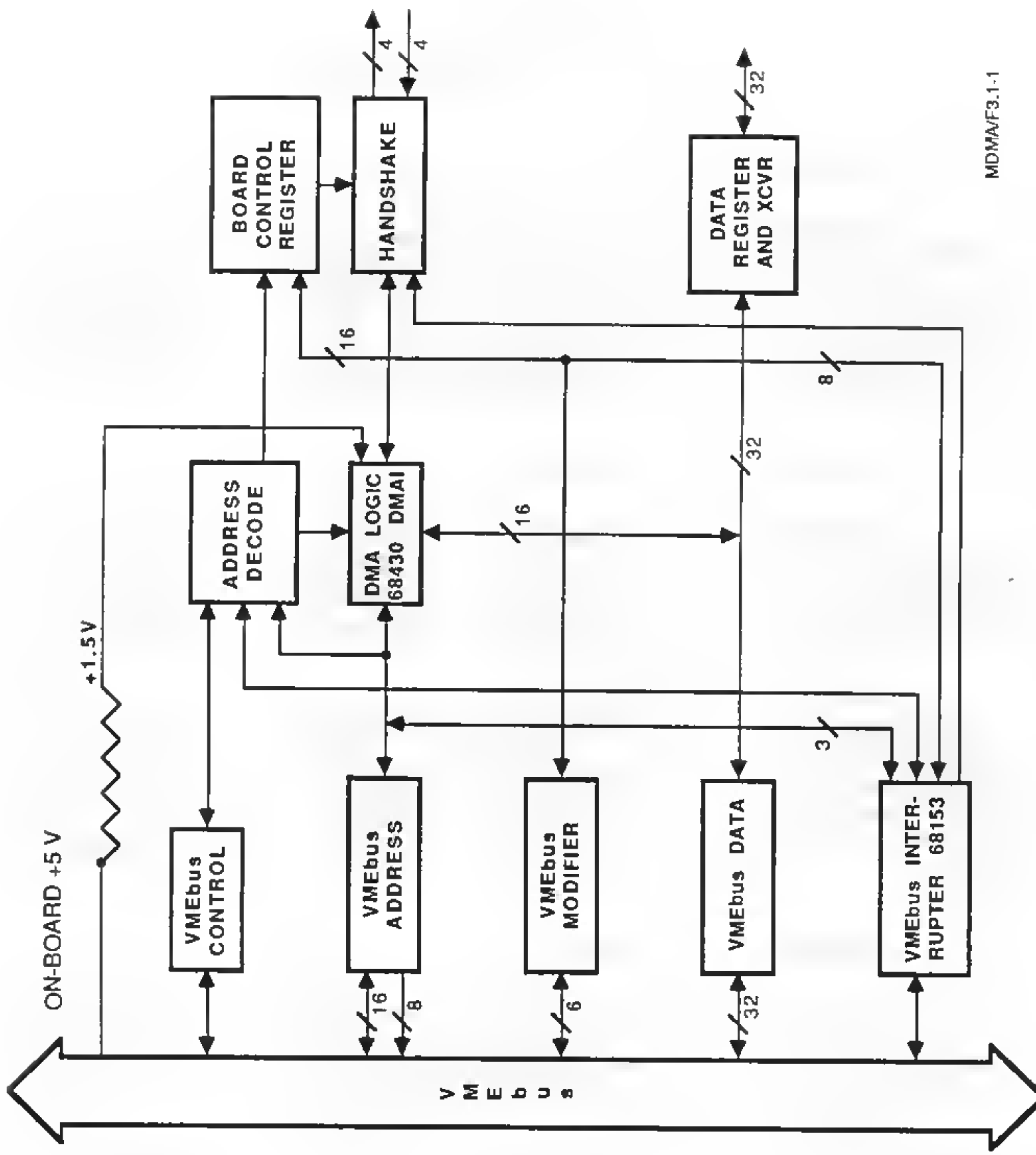
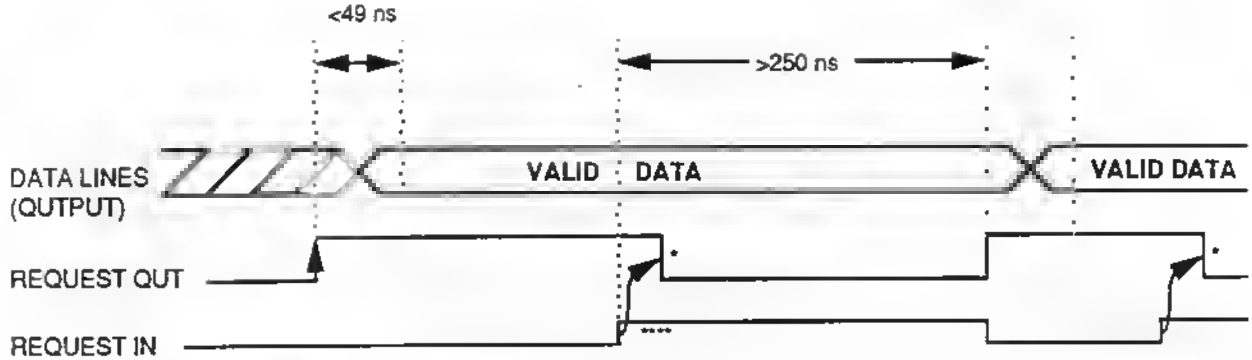


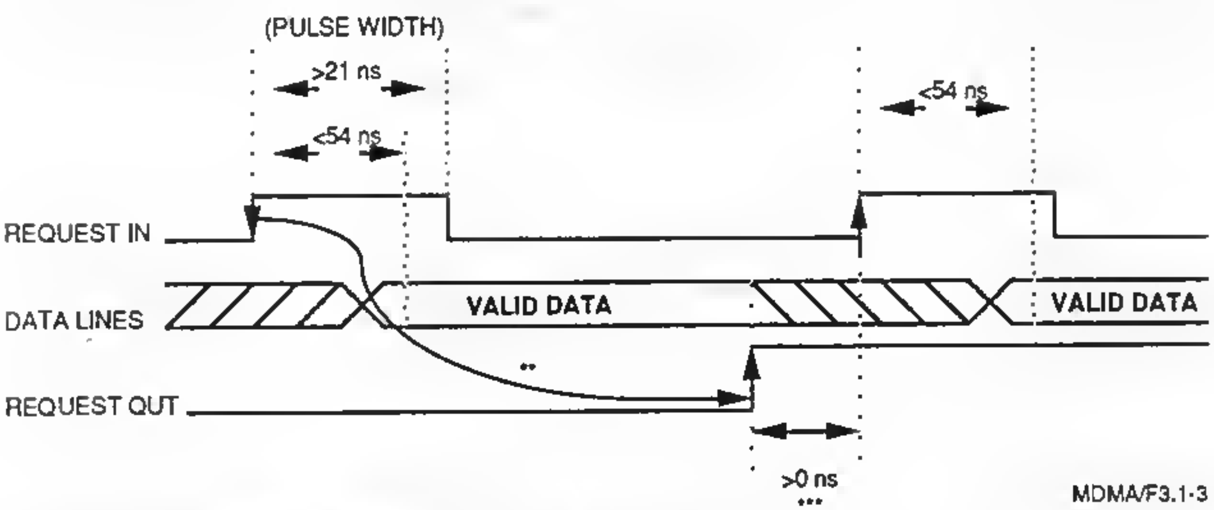
Figure 3.1-1. VMIVME-DMA Functional Block Diagram



*The rising edge of REQUEST IN clears REQUEST OUT.

**** Do Not Assert REQUEST IN until >250ns after TRANSMIT CMD goes LOW.

Figure 3.1-2. Timing for Output Data Transfers



**Rising edge of REQUEST IN initiates the rising edge of REQUEST OUT.

***Do not assert REQUEST IN until the prior data word has been acknowledged by a positive edge on the REQUEST OUT line.

Figure 3.1-3. Timing for Input Data Transfers

One protocol type would consist of the following:

a. CPU in one bus interrupts the second bus.
b. Both DMA interfaces are set up to transfer a control data block.
c. The control data block is then used to setup the DMA interface in the second bus. This protocol would simply have to insure in advance what the size and direction of transfer of the control block would be.

A second protocol type would consist of using predetermined transfer blocks and sizes and sequences. A third protocol type would consist of sending the DMA setup data via a serial communication link.

3.4 DATA TRANSFER DESCRIPTION

When the VMIVME-DMA transfers individual data works to or from an external device, it becomes the VMEbus master and transfers the data via DMA transfers to or from memory. It asserts the VMEbus address, control lines, address modifier, and sends or receives data. The data transfers are controlled by a 68430 DMA interface integrated circuit (IC). Handshake signals to/from the 68430 are converted to/from DMA compatible handshake signals. A functional block diagram of the DMA interface handshake signals is shown in Figure 3.4-1.

3.5 VME-TO-VME LINK

Two VMIVME-DMA boards may be connected back-to-back to create a DMA link between two VME chassis. In this configuration, the two boards are connected so that their data buses and control signals are cross coupled to allow them to transfer data back and forth under handshake control. The cross coupling is shown in Figure 3.4-1.

The DMA link supports 8-, 16-, and 32-bit data transfers in either burst or single cycle mode. Burst mode operation provides for maximum data transfer speeds; however, other bus masters are prohibited from bus access for the entire data transfer block. Single cycle mode relinquishes the bus after each data cycle, allowing other master devices use of the bus during data transfer blocks.

3.6 POWER CIRCUITS

The SBC 68430 DMA Controller integrated circuit utilizes a 1.5 V (VBB) power source which is derived from the VMEbus +5 V logic supply, as shown in Figure 3.6-1.

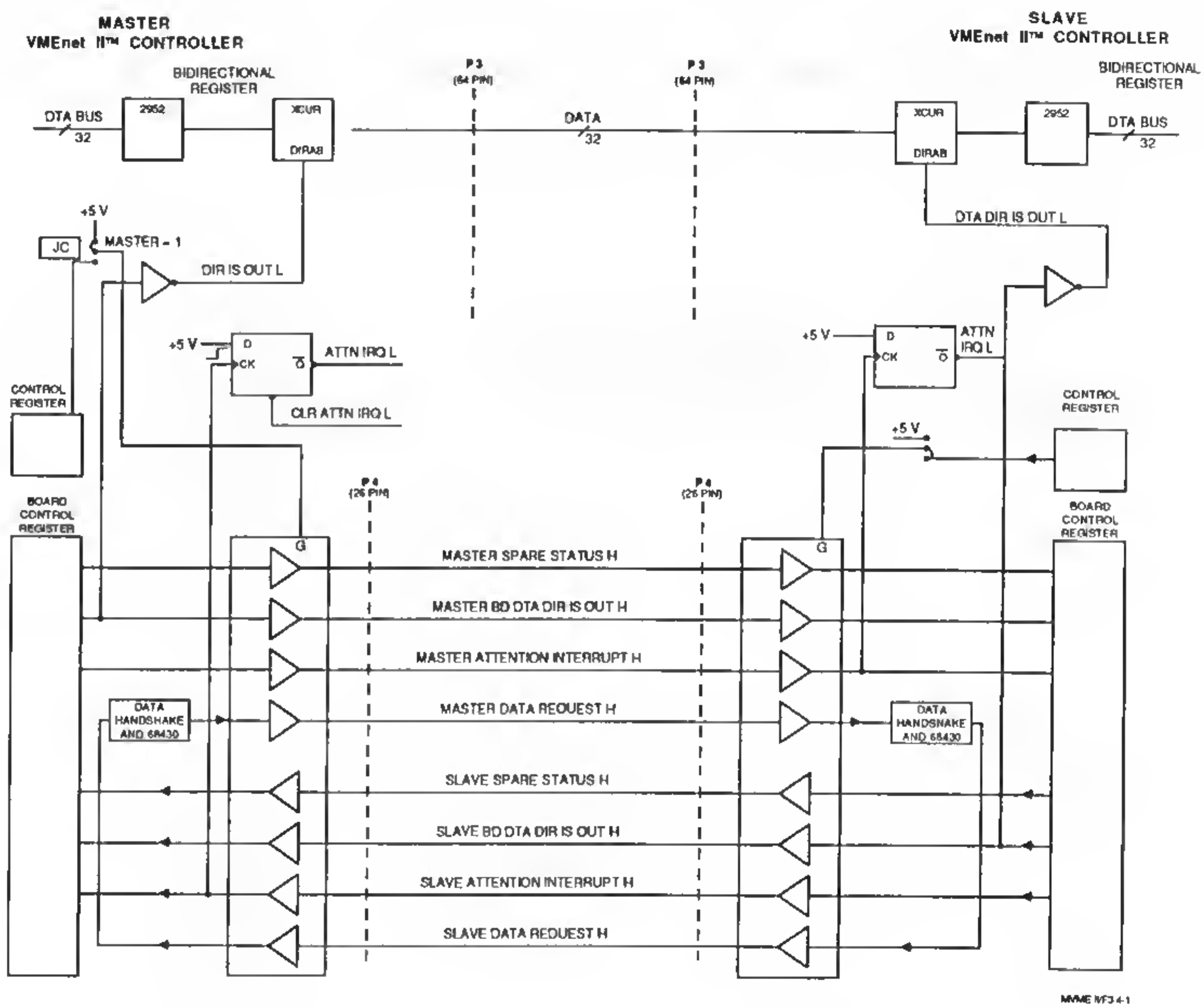


Figure 3.4-1. Functional Block Diagram of DMA Interface Signals

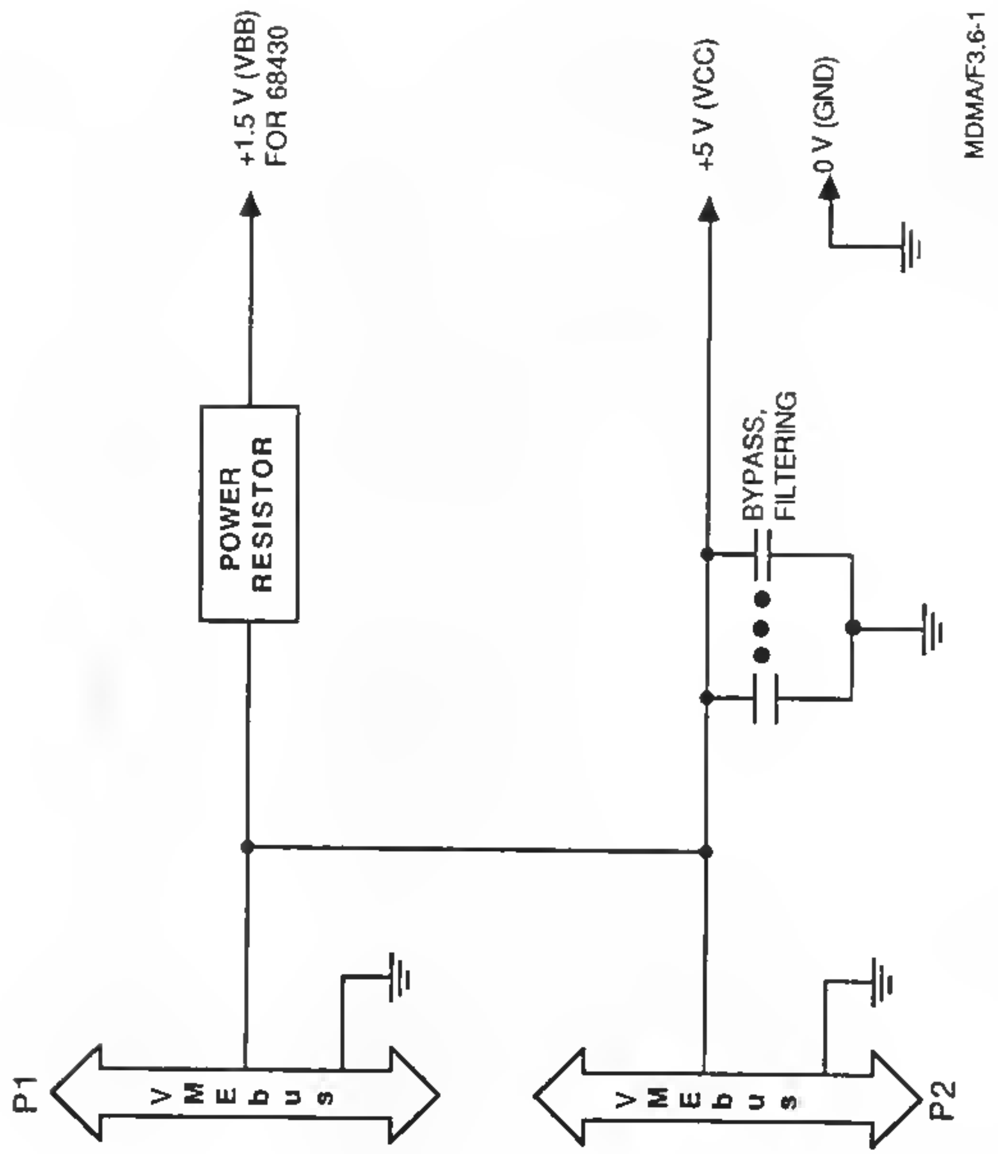


Figure 3.6-1. VMIVME-DMA Power Section Functional Block Diagram

3.7 VMEbus COMPATIBILITY LOGIC

Typical VMEbus compatible signals, buffers, and receivers are shown in Figures 3.7-1, 3.7-2, 3.7-3, and 3.7-4 for VMEbus controls, addresses, and data.

3.8 INTERRUPT LOGIC

The DMA interrupt logic consists of an interrupt vector used for a DMA complete signal that is resident inside the 68430 integrated circuit. Although the 68430 DMA controller supplies the interrupt vector, the 68153 bus interrupter interface provides the interrupt handshake logic. A functional block diagram of the 68430 control logic is shown in Figure 3.7-2.

3.9 SIGNAL FUNCTIONAL DESCRIPTIONS

This section describes the cable interface signals used by the VMIVME-DMA.

3.9.1 ED00-ED31 - Data Bus

These 32 lines make up the data bus. Data is transferred bidirectionally (half duplex) over these lines. The data is TTL compatible, terminated by 120 ohms.

3.9.2 I/O Cable Handshake Signals

When a VMIVME-DMA is selected as the A (i.e., Master) board, the *Master Signals* are driven and the *Slave Signals* are received. Whereas, when a board is selected as the B (i.e., Slave) board, then the transceivers are reversed and the *Slave Signals* are driven and the *Master Signals* are received.

3.9.2.1 Cable Handshake "Master Signals"

The following four signals are driven by the VMIVME-DMA selected as the A (Master) board:

Master Spare Status H. This signal is a user-defined output from the Master (A) board.

Master Transmit CMD. This signal indicates the transfer direction of the VMIVME-DMA. It may be read by the Board Control Register (BCR) of the other VMIVME-DMA or user device.

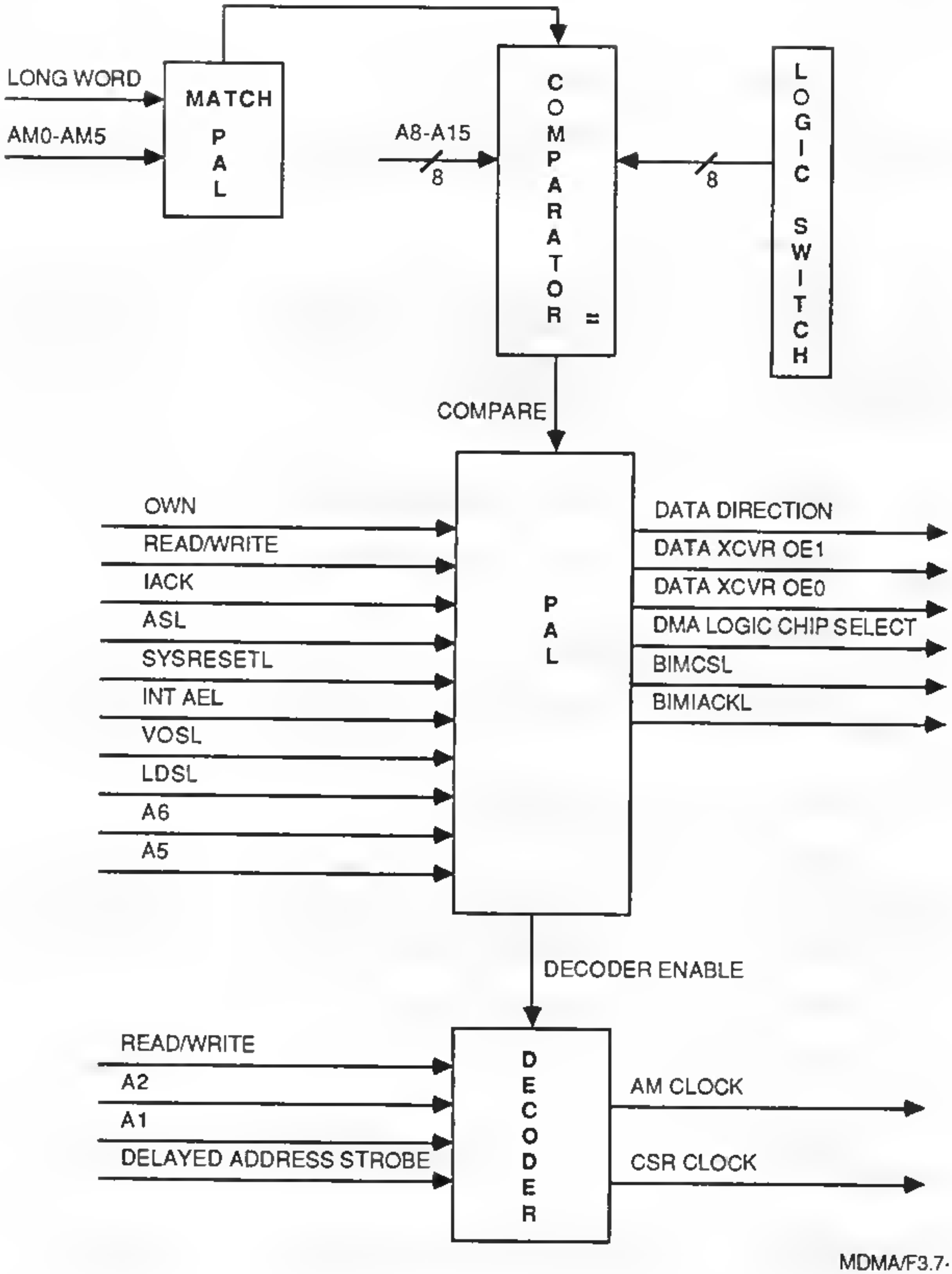


Figure 3.7-1. VMIVME-DMA Address Decode Section Detailed Block Diagram

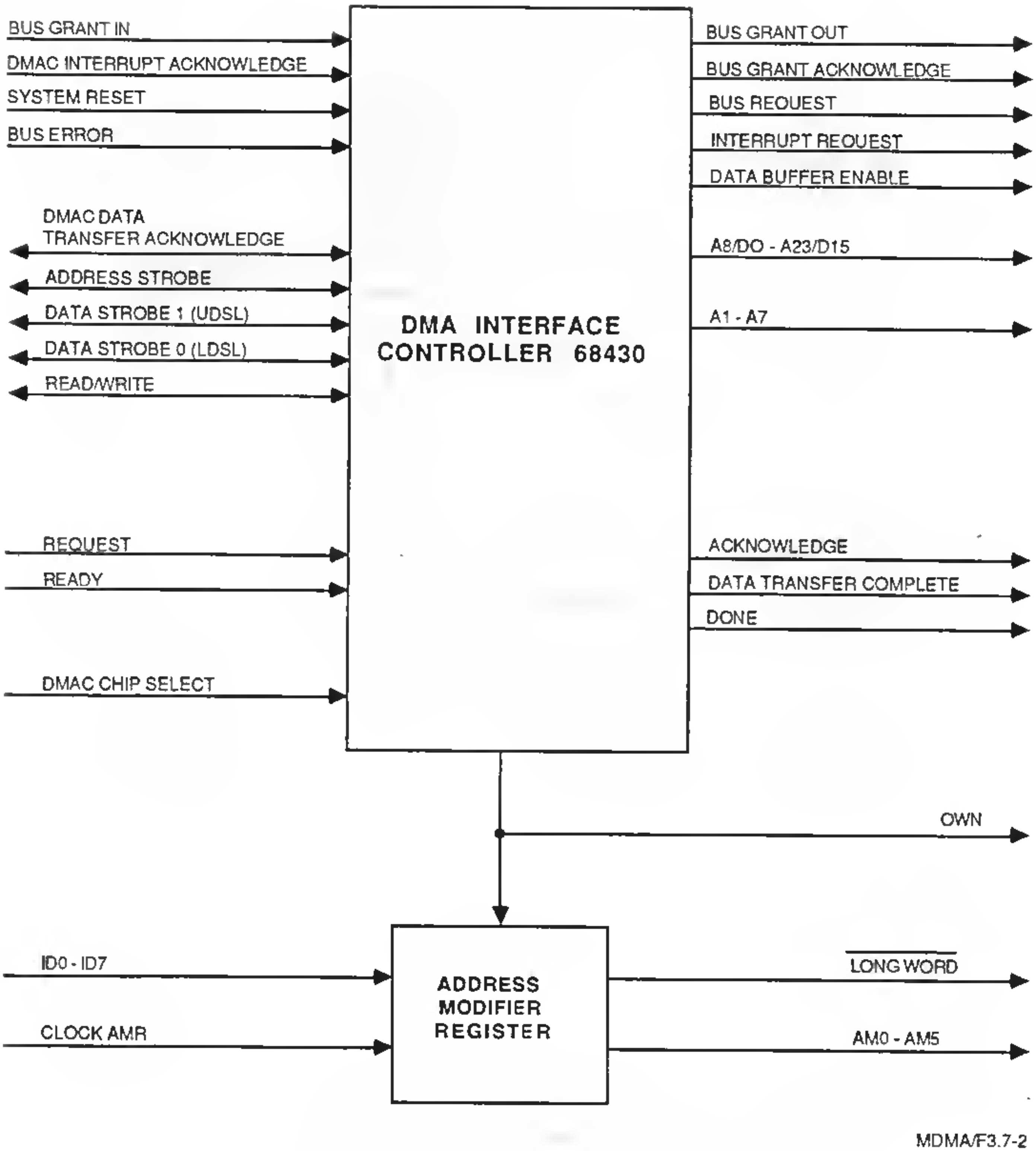


Figure 3.7-2. VMIVME-DMA Functional Block Diagram

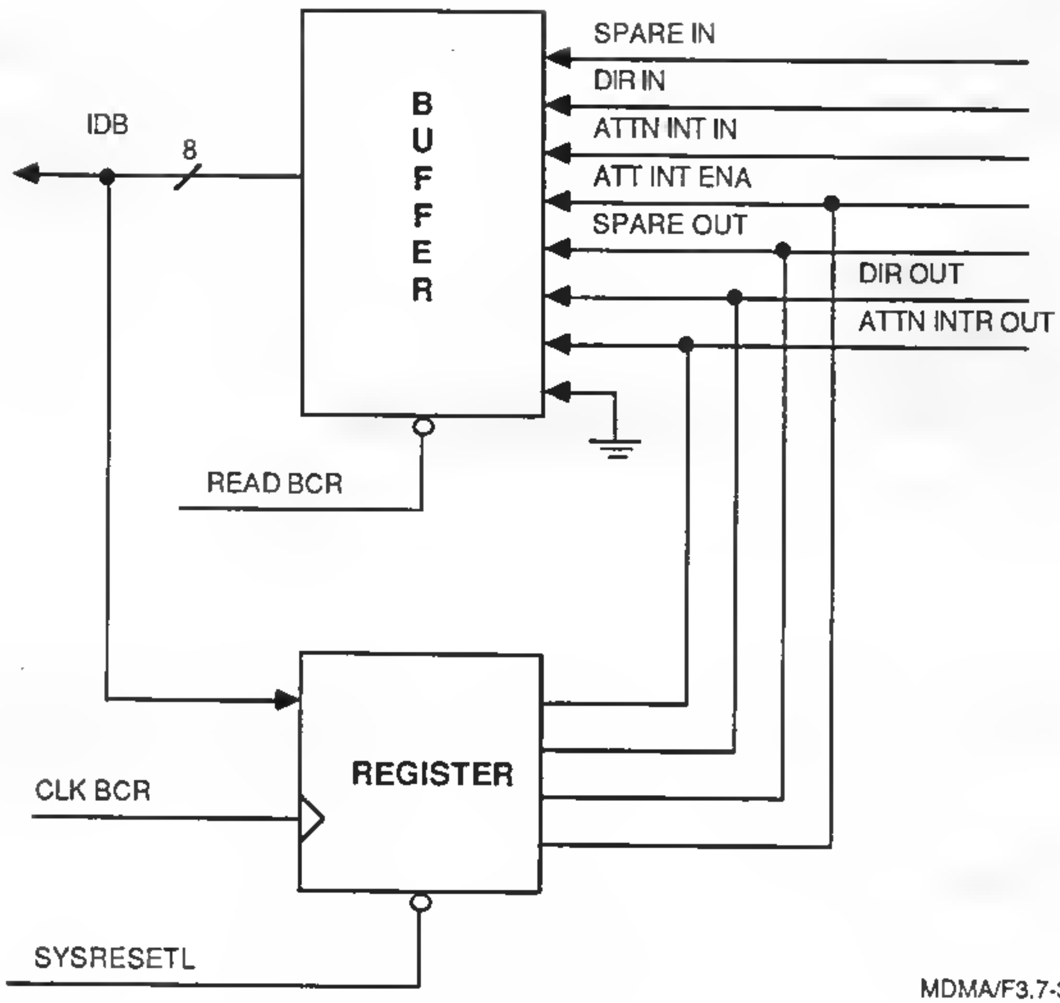


Figure 3.7-3. VMIVME-DMA Board Control Register Logic

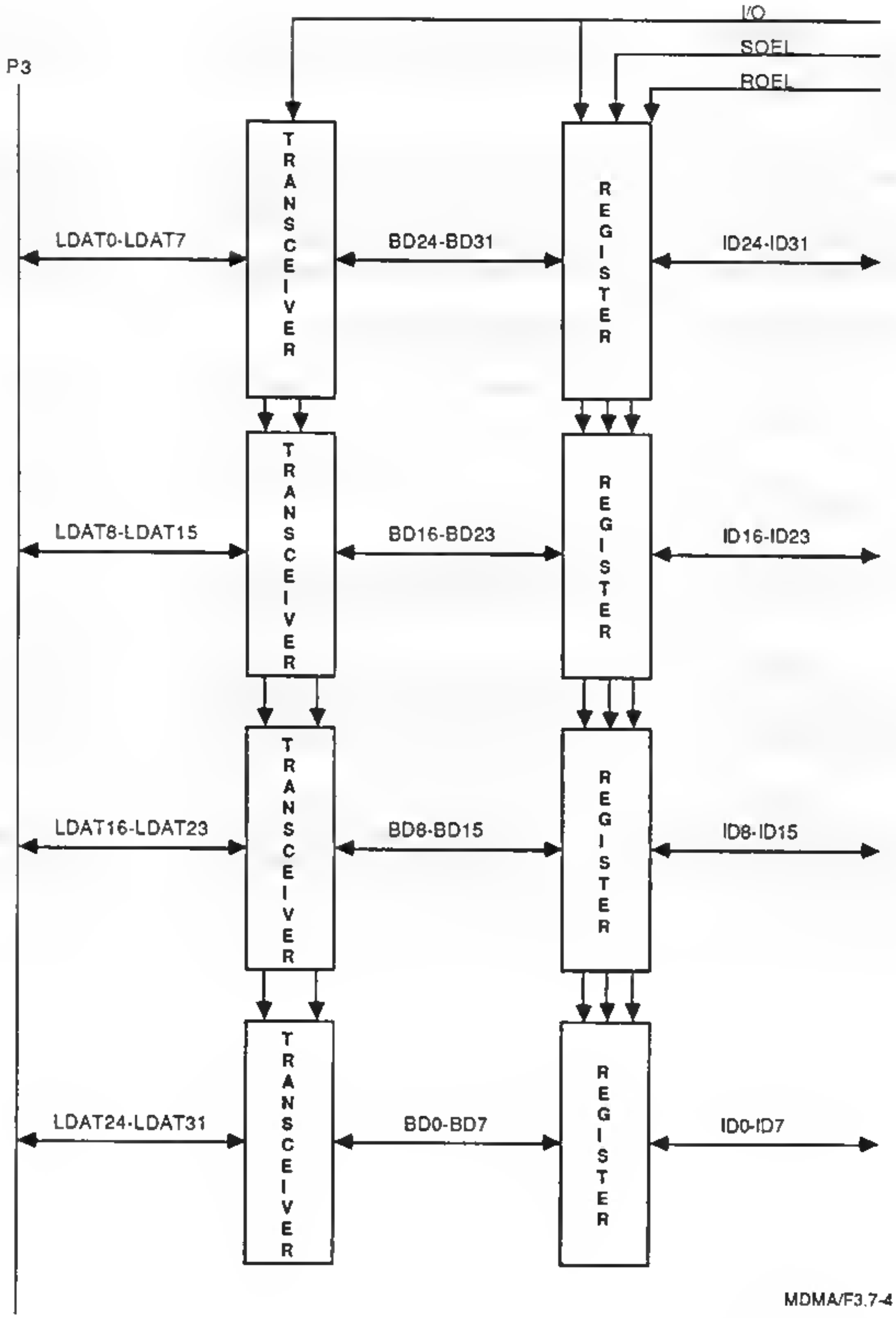


Figure 3.7-4. VMIVME-DMA Data Section Detailed Block Diagram

Master Attn Interrupt H. This signal is controlled by the *attention interrupt out* bit in the BCR. It is pulsed high to cause an *interrupt* in the user device or other VMIVME-DMA.

Master Request H. This signal is the request output which requests a DMA cycle on the other interface. When a DMA cycle is started MASTER DTA REQUEST is NEGATED, and after the cycle is completed it goes back high, therefore, requesting a cycle on the other interface. The REQUEST signals form a handshake interlock between the two interfaces during transfer of data blocks.

3.9.2.2 Cable Handshake "Slave Signals"

The following signals are driven by the VMIVME-DMA selected as the B (Slave) board:

Slave Spare Status H. This signal is a user-defined input to the Master (A) board.

Slave Bd Transmit CMD H. This input signal indicates the state of the data direction bit in the Slave (B) VMIVME-DMA or user device.

Slave Attn Interrupt H. This signal allows the Slave (B) VMIVME-DMA or user device to cause an interrupt if the ATTN INTR ENABLE bit is set in the BCR (on the Master (A) board) and if the Bus Interrupter Module (BIM) is programmed correctly. The interrupt occurs on the positive edge of this signal.

Slave Request H. This signal Is the data transfer request input to the Master (A) DMA controller. The positive edge of this signal indicates that input data is ready or that another output word is needed. The negative edge of this signal indicates that the input data was received and no output word is needed.

SECTION 4

PROGRAMMING

4.1 PROGRAMMING OVERVIEW

The VMIVME-DMA has three types of devices that must be programmed for proper operation. These are the SCB68430 DMA Controller, the MC68153 Bus Interrupter Module (BIM), and the on-board registers. The on-board registers are used to provide the address modifiers, which allows the user control of the DMA controller and the Bus Interrupter Module, and to communicate with the external DMA devices or another DMA board connected back-to-back for VMEbus-to-VMEbus communications. Other programming aspects of the DMA include executing the transfer protocol (see Section 4.1.2), handling interrupts, and error processing. See Table 4.1-1 for names and addresses of registers utilized by the DMA. Technical specifications for the MC68153 are included in Appendix B.

4.1.2 Transfer Protocol

In order for DMA transfers to take place, the interfaces must be set up at both ends of the link. Therefore, if a CPU on one bus wants to transfer data, a second CPU on the second bus must set up the DMA interface on that second bus to the correct memory address, word count, and direction of transfer.

The manner in which CPUs in two separate buses determine the proper setup sequences is referred to as the transfer protocol. There are several types of protocols that may be used. One protocol type consists of the following:

a. CPU in one bus interrupts the second bus.
b. Both DMA interfaces are set up to transfer a control data block.
c. The control data block is then used to set up the DMA interface in the second bus. This protocol would simply have to insure in advance what the size and direction of transfer of the control block would be.

A second protocol type consists of using predetermined transfer blocks, sizes, and sequences. A third protocol type consists of sending the DMA setup data via a serial communication link.

4.2 REGISTER BIT DEFINITIONS

Register Bit definitions are shown in Tables 4.2-1, 4.2-2, and 4,2-3.

Table 4.1-1. VMIVME-DMA Register Address Map

ADDRESS	ACRONYM	REGISTER NAME	PHYSICAL LOCATION
00	CSR	Channel Status Register (CSR)	SCB68430 DMAI
01	CER	Channel Error Register (CER)	SCB68430 DMAI
04	DCR	Device Control Register (DCR)	SCB68430 DMAI
05	OCR	Operation Control Register (OCR)	SCB68430 DMAI
06	SCR*	Sequence Control Register (SCR)	SCB68430 DMAI
07	CCR	Channel Control Register (CCR)	SCB68430 DMAI
0A	MTCH	Memory Transfer Count High	SCB68430 DMAI
0B	MTCL	Memory Transfer Count Low	SCB68430 DMAI
0C	MACH**	Memory Address Count High	SCB68430 DMAI
0D	MACMH	Memory Transfer Count Mid-High	SCB68430 DMAI
0E	MACML	Memory Address Count Mid-Low	SCB68430 DMAI
0F	MACL	Memory Address Count Low	SCB68430 DMAI
25	IVR	Interrupt Vector Register	SCB68430 DMAI
27	IVR***	Interrupt Vector Register	SCB68430 DMAI
2D	CPR*	Channel Priority Register	SCB68430 DMAI
41	CRO**	Control Register 0	MC68153 BIM
43	CR1**	Control Register 1	MC68153 BIM
45	AICR (CR2)	Attention Interrupt Control Register	MC68153 BIM
47	DICR (CR3)	DMA Interrupt Control Register	MC68153 BIM
49	VRO**	Vector Register 0	MC68153 BIM
4B	VR1**	Vector Register 1	MC68153 BIM
4D	AIVR (VR2)	Attention Interrupt Vector Register	MC68153 BIM
4F	VR3**	Vector Register 3	MC68153 BIM
61	BCR	Board Control Register	
63	DSR	Device Status Register	(On Board)
65	AMR	Address Modifier Register	

MOMA/T4.1-1

* Included for software compatibility.
** Register is not used.
*** The IVR has two addresses for software compatibility (see specification sheet).

Table 4.2-1. DMA Interface Register Bit Formats

CHANNEL STATUS REGISTER (ADDRESS: $XX00)

	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
CSR	CHANNEL OPERATION COMPLETE	NOT USED	NORMAL DEVICE TERMINATE	ERROR	CHANNEL ACTIVE	NOT USED	NOT USED	READY INPUT STATE
	0 = NO 1 = YES	(0)	0 = NO 1 = YES	0 = NO 1 = YES	0 = NO 1 = YES	(0)	(0)	0 = LOW 1 = HIGH

CHANNEL ERROR REGISTER ($XX01)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CER	NOT USED	NOT USED	NOT USED	ERROR CODE				
	(0)	(0)	(0)	0000 = NO ERROR 01001 = BUS ERROR 10001 = SOFTWARE ABORT				

DEVICE CONTROL REGISTER ($XX04)

	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11*	BIT 10	BIT 9	BIT 8
DCR	EXTERNAL REQUEST MODE	NOT USED	NOT USED	NOT USED	OCR (5:4) = 00 → 0	NOT USED	NOT USED	NOT USED
	0 = BURST 1 = CYCLE STEAL	(0)	(1)	(1)	OCR (5:4) 01 10 } → 1 11	(0)	(0)	(0)

*Should be programmed as a logical "zero" if the operand size (see Operation Control Register bits 4 and 5) is BYTE, otherwise it should be programmed as a logic "one".

OPERATION CONTROL REGISTER ($XX05)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OCR	DIRECTION	NOT USED	OPERAND SIZE		NOT USED	NOT USED	NOT USED	NOT USED
	0 = MEM TO DEV 1 = DEV TO MEM	(0)	00 = BYTE 01 = WORD 10 = LONG WORD* 11 = 32-BIT WORD		(0)	(0)	(1)	(0)

*Do not select Longword transfers for this board.

MDMA/T4.2-1/1

Table 4.2-1. DMA Interface Register Bit Formats (Continued)

SEQUENCE CONTROL REGISTER ($XX06)

	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
SCR**	NOT USED**							
	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

**Dummy register.

CHANNEL CONTROL REGISTER ($XX07)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CCR	START	NOT USED	NOT USED	SOFTWARE ABORT	INTERRUPT ENABLE	NOT USED	NOT USED	NOT USED
	0 = NO 1 = YES	(0)	(0)	0 = NO 1 = YES	0 = NO 1 = YES	(0)	(0)	(0)

MEMORY TRANSFER COUNT HIGH ($XX0A)

	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
MTCH	MEMORY TRANSFER COUNT MSB							
	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8

MEMORY TRANSFER COUNT LOW ($XX0B)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MTCL	MEMORY TRANSFER COUNT LSB							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

MSIU/T4.2-1/2

Table 4.2-1. DMA Interface Register Bit Formats (Continued)

MEMORY ADDRESS COUNTER HIGH ($XX0C)

	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
MACH	NOT USED**							
	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

**Dummy register.

MEMORY ADDRESS COUNTER MID-HIGH ($XX0D)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MACMH	MEMORY ADDRESS COUNTER							
	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16

MEMORY ADDRESS COUNTER MID-LOW ($XX0E)

	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
MACML	MEMORY ADDRESS COUNTER							
	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8

MEMORY ADDRESS COUNTER LOW ($XX0F)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MACL	MEMORY ADDRESS COUNTER							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

MSIU/T4.2-1/3

Table 4.2-1. DMA Interface Register Bit Formats (Concluded)

DMA INTERRUPT VECTOR REGISTER ($XX25. $XX27)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVR	DONE INTERRUPT VECTOR							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	NOTE 1

NOTE 1: This bit is automatically set if an error occurred. This register is mapped to two locations to provide compatibility with other controllers.

CHANNEL PRIORITY REGISTER ($XX2D)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CPR	NOT USED**							
	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

**Dummy registers.

MSIU/T4.2-1/4

Table 4.2-1. DMA Interface Register Bit Formats (Continued)

MEMORY ADDRESS COUNTER HIGH ($XX0C)

	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
MACH	NOT USED**							
	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

**Dummy register.

MEMORY ADDRESS COUNTER MID-HIGH ($XX0D)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MACMH	MEMORY ADDRESS COUNTER							
	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16

MEMORY ADDRESS COUNTER MID-LOW ($XX0E)

	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
MACML	MEMORY ADDRESS COUNTER							
	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8

MEMORY ADDRESS COUNTER LOW ($XX0F)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MACL	MEMORY ADDRESS COUNTER							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

MSIU/T4.2-1/3

Table 4.2-2. Interrupt Module (68153) Register Bit Definitions

ATTENTION INTERRUPT CONTROL REGISTER ($XX45)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AICR	FLAG BIT	FLAG BIT AUTO CLEAR	VECTOR 0 = INT 1 = EXT	INTER-RUPT ENABLE	INTER-RUPT AUTO CLEAR	IRQ LEVEL 2	IRQ LEVEL 1	IRQ LEVEL 0

DMA INTERRUPT CONTROL REGISTER ($XX47)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DICR	FLAG BIT	FLAG BIT AUTO CLEAR	VECTOR 0 = INT 1 = EXT	INTER-RUPT ENABLE	INTER-RUPT AUTO CLEAR	IRQ LEVEL 2	IRQ LEVEL 1	IRQ LEVEL 0

ATTENTION INTERRUPT VECTOR REGISTER ($XX4D)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AIVR	ATTENTION INTERRUPT VECTOR							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

MSIU/T4.2-2

Table 4.2-3. Registers Located External to DMAI and BIM ICs (On Board)

BOARD CONTROL REGISTER ($XX61)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BCR	SPARE IN	DIR IN	ATTN INTR IN	ATTN INTR ENABLE	SPARE OUT	DIR OUT 0 = Rx 1 = Tx	ATTN INTR OUT	GO
READ/WRITE	R	R	R	R/W	R/W	R/W	R/W	W

DEVICE STATUS REGISTER ($XX63)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DSR	FAIL LED 1 = OFF 0 = ON	NOT USED	ENABLE WATCH DOG TIMER 1 = ENA	LINK MASTER HIGH "1"	NOT USED	NOT USED	NOT USED	NOT USED
READ/WRITE	R/W	R/W	R/W	R/W	R	R	R	R

ADDRESS MODIFIER REGISTER ($XX65)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AMR	NOT USED	$\overline{\text{LONGWORD}}$	ADDRESS MODIFIER					
			AM5	AM4	AM3	AM2	AM1	AM0

MSIU/T4.2-3

4.3 SEQUENCE OF REGISTER LOADING

The DMA interface at the receiving end must be set up first to avoid missing the first cycle request, furthermore, the overall setup sequence of the VMIVME-DMA should be as follows:

a. Load the registers in the 68153 and 68430.
b. The CCR should be the last register loaded in the 68430.
c. Load the address modifier register (on-board).
d. Load the board control register (on-board) with the GO bit (bit 0) set to 0.
e. Reload the board control register with the GO bit set.

Note that the start bit (CCR bit 7) must be set inside the 68430 before the GO bit is set in the BCR. The start bit in the 68430 is independent of the GO bit in the BCR.

An example of a register re-initialization sequence for transmitting data (from memory) is shown in Table 4.3-1. After the first DMA transfer is done, the VMIVME-DMA can be re-initialized with only eight steps to transmit a second block of data (see Table 4.3-2).

An example of a register initialization sequence for receiving data (transfer to memory) is shown in Table 4.3-3. After the first DMA transfer is done the VMIVME-DMA can be initialized with only eight steps to receive a second block of data (see Table 4.3-4).

4.4 PROGRAMMING THE SCB68430 DMAI

The following paragraphs describe the functions of the internal registers to the DMAI chip.

4.4.1 Channel Status Register/Channel Error Register

These two registers are used together to determine status and error conditions related to the DMA controller.

4.4.1.1 Channel Status Register (CSR)

BIT 15 - CHANNEL OPERATION COMPLETE. This bit will be set when the DMA operation is complete. If interrupts are enabled, an interrupt will be generated at this time.

BITS 14, 13 - NOT USED.

Table 4.3-1. Register Initialization Sequence for Transmitting a 4K Word Block Starting Data Address $40000

STEP	REGISTER LOCATION	REGISTER NAME	REGISTER ADDRESS OFFSET	DATA LOADED (HEXADECIMAL)	COMMENT
1	68430	DCR	04	B8	CYCLE STEAL
2	68430	OCR	05	12	WORD FROM MEMORY
3	68430	MTCH	0A	1000	16-BIT TRANSFER COUNT
4	68430	MACMH	0D	04	UPPER 8-BITS OF MEMORY ADDRESS
5	68430	MACML	0E	0000	LOWER 16-BITS OF MEMORY ADDRESS
6	68430	DIVR	25	42	DONE INTERRUPT VECTOR
7	68153	AIVR	4D	40	ATTENTION INTERRUPT VECTOR
8	68153	AICR	45	1F	ENABLE INTERNAL VECTOR WITH AUTO CLEAR
9	68153	DICR	47	3F	ENABLE EXTERNAL VECTOR WITH AUTO CLEAR
10	ON-BOARD	AMR	65	39	LONGWORD, ADDR MOD=39
11	68430	CSR	00	B9	CLEAR CHANNEL STATUS REGISTER
12	68430	CCR	07	88	START DMA CHIP
13	ON-BOARD	DSR	63	80	FAIL LED OFF
14	ON-BOARD	BCR	61	15	GO, ENABLE ATTN, TRANSMIT OUT

MSIU/T4.3-1

Table 4.3-2. Register Initialization Sequence for Transmitting a Second 4K Word Block Starting Data Address $20000

STEP	REGISTER LOCATION	REGISTER NAME	REGISTER ADDRESS OFFSET	DATA LOADED (HEXADECIMAL)	COMMENT
1	68430	MTCH	0A	1000	16-BIT TRANSFER COUNT
2	68430	MACMH	0D	02	UPPER 8-BITS OF MEMORY ADDRESS
3	68430	MACML	0E	0000	LOWER 16-BITS OF MEMORY ADDRESS
4	68153	DICR	47	3F	ENABLE INTERRUPTS WITH AUTO CLEAR
5	68430	CSR	00	B9	CLEAR CHANNEL STATUS REGISTER
6	68430	CCR	07	88	START DMA CHIP
7	ON-BOARD	DSR	63	80	FAIL LED OFF
8	ON-BOARD	BCR	61	15	GO, ENABLE ATTN, TRANSMIT OUT

MSIU/T4.3-2

Table 4.3-3. Register Initialization Sequence for Receiving a 4K Word Block Starting Data Address $40000

STEP	REGISTER LOCATION	REGISTER NAME	REGISTER ADDRESS OFFSET	DATA LOADED (HEXADECIMAL)	COMMENT
1	68430	DCR	04	B8	CYCLE STEAL
2	68430	OCR	05	92	WORD TO MEMORY
3	68430	MTCH	0A	1000	16-BIT TRANSFER COUNT
4	68430	MACMH	0D	04	UPPER 8-BITS OF MEMORY ADDRESS
5	68430	MACML	0E	0000	LOWER 16-BITS OF MEMORY ADDRESS
6	68430	DIVR	25	42	DONE INTERRUPT VECTOR
7	68153	AIVR	4D	40	ATTENTION INTERRUPT VECTOR
8	68153	AICR	45	17	ENABLE INTERNAL VECTOR WITH AUTO CLEAR
9	68153	DICR	47	3F	ENABLE EXTERNAL VECTOR WITH AUTO CLEAR
10	ON-BOARD	AMR	65	39	LONGWORD, ADDR MODE = 39
11	68430	CSR	00	B9	CLEAR CHANNEL STATUS REGISTER
12	68430	CCR	07	88	START DMA CHIP
13	ON-BOARD	BCR	61	10	GO = 0, ENABLE ATTN, RECEIVE
14	ON-BOARD	DSR	63	80	FAIL LED OFF
15	ON-BOARD	BCR	61	11	GO, ENABLE ATTN, RECEIVE

MSIU/T4.3-3

Table 4.3-4. Register Initialization Sequence for Receiving a Second 4K Word Block Starting Data Address $20000

STEP	REGISTER LOCATION	REGISTER NAME	REGISTER ADDRESS OFFSET	DATA LOADED (HEXADECIMAL)	COMMENT
1	68430	MTCH	0A	1000	16-BIT TRANSFER COUNT
2	68430	MACMH	0D	02	UPPER 8-BITS OF MEMORY ADDRESS
3	68430	MACML	0E	0000	LOWER 16-BITS OF MEMORY ADDRESS
4	68153	DICR	47	3F	ENABLE INTERRUPTS WITH AUTO CLEAR
5	68430	CSR	00	B9	CLEAR CHANNEL STATUS REGISTER
6	68430	CCR	07	88	START DMA CHIP
7	ON-BOARD	DSR	63	80	FAIL LED OFF
8	ON-BOARD	BCR	61	15	GO, ENABLE ATTN, RECEIVE

MSIU/T4.3-4

BIT 12 - ERROR.* This bit will be set if the DMA operation was terminated due to an error condition.

BIT 11 - CHANNEL ACTIVE. This bit indicates that a DMA operation is in progress and is automatically cleared upon termination of the operation.

BITS 10, 9 - NOT USED.

BIT 8- READY INPUT. Indicates the state of the RDY input signal, i.e., a logic "zero" indicates 0 Volts and that data is ready.

4.4.1.2 Channel Error Register (CER)

BITS 7, 6, 5 - NOT USED.

BIT 4, 3, 2, 1, 0 ERROR CODE. These five bits indicate the error type when an error occurs. This register is cleared when the error bit (CSR-BIT 12) is cleared.

ERROR CODE	FUNCTION
00000	No Error
01001	Bus Error
10001	Software Abort

4.4.2 Device Control Register/Operation Control Register

These two registers control the data direction, data size, and request mode of the DMA transfers.

4.4.2.1 Device Control Register (DCR)

BIT 15 - EXTERNAL REQUEST MODE. This bit is set to perform single-cycle transfers and cleared to perform burst transfers.

*CSR-BIT 15 and CSR-BIT 12 must be cleared if set before another DMA operation can be started. These bits may be cleared by writing a "one" to each bit that is set. The following 68000 instruction will do this without testing each of the bits.

```
MOVE.B     CSR, CSR
```

The other bits in the CSR are unaffected by a write.

BITS 14, 13, 12 - NOT USED.

BIT 11 - SIZE. This bit is read and written as the "LOGICAL OR" of bits 4 and 5 in the OCR, i.e., set it to "zero" if both bits 4 and 5 are zero (otherwise, set it to "one").

BITS 10, 9, 8 - NOT USED.

4.4.2.2 Operation Control Register (OCR)

BIT 7 - DIRECTION. This bit contains the DMA transfer direction.

0=Read from Memory
  Write to External Device
1=Write to Memory
  Read from External Device

BIT 6 - NOT USED.

BITS 5, 4 OPERAND SIZE. These bits control the operand size.

BIT 5	BIT 4	OPERAND SIZE
0	0	BYTE
0	1	WORD (16-bit)
1	0	LONGWORD* (32-bit, 16 bits at a time)
1	1	DOUBLEWORD (32-bit, 32 bits at a time)

*For maximum bus efficiency, select the doubleword size. Do not use LONGWORD with this board.

BITS 3, 2, 1, 0 - NOT USED.

4.4.3 Sequence Control Register (SCR)

The SCR is a dummy register provided for compatibility with other DMA controllers.

4.4.4 Channel Control Register (CCR)

BIT 7 - START. This bit causes the DMA controller to start its operation.

BITS 6, 5 - NOT USED.

BIT 4 - SOFTWARE ABORT. This bit allows current DMA operation to be aborted under software control.

BIT 3 - INTERRUPT ENABLE. This bit enables the DMA interrupt request when a DMA operation is completed.

BIT 2, 1, 0 - NOT USED.

4.4.5 Memory Transfer Count Register

These registers hold the number of desired transfers for the current operation. The transfer count can be set to FFFF (64k-1) if the VMIVME-DMA is in the slave mode. The Last Word Flag (LWF) signal is used to terminate the transfers in this case. However, setting the transfer counter to FFFF does cause an extra memory cycle to be requested beyond the actual word count (only if a *read* from memory). This should not be a problem unless it happens to be at the end of memory, in that case it will generate a bus error trap.

4.4.6 Memory Address Counter Registers

These four registers hold the memory address for the DMA operation. The MACH register is a dummy register and is provided for compatibility with other DMA controllers. The three real registers provide a 24-bit memory address for the DMA transfers. These registers should be loaded with the starting memory address before an operation is started. The registers are incremented during operation and may be read while an operation is in progress.

4.4.7 DMA Interrupt Vector Register (DIVR)

This register is used to store the interrupt vector used for the DMA complete interrupt. This register is resident inside the SCB68430. It is mapped to two locations to provide compatibility with other DMA controllers. Note: Bit 0 is automatically set when an error occurs and cannot be written. Thus, a DMA interrupt vector for normal conditions must be an even number, and the error vector is automatically the next higher odd vector. Note, that although the 68430 supplies the interrupt vector, the 68153 handles the interrupt handshake, therefore, the 68153 must be programmed to handle the external vector from the 68430.

4.4.8 Channel Priority Register (CPR)

This register is a dummy register provided for compatibility with other DMA controllers.

4.5 PROGRAMMING THE MC68153 BIM

Data sheets for the MC68153 are included in Appendix B. The MC68153 contains eight registers, but only three are used in the VMIVME-DMA. Two of these registers are control registers and one is a vector register.

4.5.1 Attention Interrupt Control Register (AICR) and DMA Interrupt Control Register (DICR)

BITS 7, 6 - FLAG CONTROL - NOT USED.

BIT 5 - VECTOR LOCATION. This bit should be cleared to cause the MC68153 to use its internal vector register for an interrupt acknowledge and set to use an external interrupt vector. For the VMIVME-DMA, this bit should be cleared in the a AICR and set in the DICR since an external vector is obtained from the 68430 DMA controller vector register (DIVR).

BIT 4 - INTERRUPT ENABLE. This bit should be set to enable the corresponding interrupt.

BIT 3 - INTERRUPT AUTO CLEAR. This bit automatically clears the interrupt enable bit and the interrupt request output whenever the interrupt is acknowledged. This bit ***MUST*** be set in both registers to provide VMEbus compatible timing. This requires that the interrupt enable bit be set after each interrupt.

BITS 2,1,0 - IRQ LEVEL BITS. Interrupt level (L2,L1,L0) - The least significant 3-bit field of the register determines the level at which an interrupt will be generated:

L2	L1	L0	IRQ LEVEL
0	0	0	DISABLED*
0	0	1	IRQ1
0	1	0	IRQ2
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

*A value of zero in the field disables the interrupt.

4.5.2 Attention Interrupt Vector Register (AIVR)

This register holds the vector used for the attention interrupt. Any 8-bit integer may be used as determined by the system vector address configuration.

4.6 PROGRAMMING THE ON-BOARD REGISTERS

4.6.1 Board Control Register (BCR)

BIT 7 - SPARE IN (READ ONLY). This bit provides the state of the SPARE IN line. Its function is user defined.

BIT 6 - DIR IN (DIRECTION INPUT; READ ONLY). This bit simply indicates the state of the SPARE IN line. When communicating with another VMIVME-DMA, it should be the complement of DIR OUT.

DIR IN	OTHER VMIVME-DMA FUNCTION
0	Other Interface is a Receiver
1	Other Interface is a Transmitter

BIT 5 - ATT INTR IN (ATTENTION INTERRUPT INPUT; READ ONLY). This bit provides the state of the ATTN INTR IN line. It allows polling or user definition of the ATT INTR line.

BIT 4 - ATT INT ENA (ATTENTION INTERRUPT ENABLE; READ/WRITE). This bit, when set, enables the attention interrupt flip-flop. This bit must be set in addition to the AICR-BIT 4 to allow attention interrupts.

BIT 3 - SPARE OUT (WRITE/READ). This bit drives the SPARE OUT line. Its function is user defined.

BIT 2 - DIR OUT (DIRECTION OUTPUT; WRITE/READ). This bit indicates the transfer direction to the other interface via the DIR OUT line. It also controls the transfer direction of the data transceivers.

DIR OUT	FUNCTION
0	Receive Data From Other Interface
1	Transmit Data to Other Interface

BIT 1 - ATT INT OUT (ATTENTION INTERRUPT OUTPUT). This bit controls the ATT INT OUT line. It should be toggled high and then low to interrupt the other VMIVME-DMA.

BIT 0 - GO (WRITE ONLY). This bit "primes" the handshake logic to start a transfer block. If transmitting, it also initiates the first DMA cycle.

4.6.2 Device Stetus Register (DSR)

BIT 7 - Fail LED. This bit controls the Fail LED. Settling this bit to a "one" turns the Fail LED OFF.

BIT 6 - NOT USED.

BIT 5 - WATCHDOG TIMER ENABLE. This bit must be set to a "one" in conjunction with the removal of the WDT jumper to enable the watchdog timer (see Section 5.3.3). Writing a "zero" disables the watchdog timer.

BIT 4 - LINK MASTER HIGH. Setting this bit to a logic "one" sets the board as Link Master A. The board may also be jumpered as Link Master A as shown in Table 5.3.2-1. This bit set to a "zero" at power-up and at reset (Link Slave B). See Table 5.3.2-1.

BITS 3, 2, 1, 0 - NOT USED.

4.6.3 Address Modifier Register (AMR)

This register contains the address modifier and longword bits which are asserted when the VMIVME-DMA is bus master. This register is write only.

BIT 7 - NOT USED.

BIT 6 - $\overline{\text{LONGWORD}}$. This bit controls the assertion of the VMEbus LWORDL signal and selects either 16 or 32-bit transfers.

$\overline{\text{LONGWORD}}$	TRANSFER SIZE
0	32-Bit
1	8 or 16-Bit

BITS 5, 4, 3, 2, 1, 0 ADDRESS MODIFIER BITS. See "The VMEbus Specification" for VMEbus address modifier codes.

4.7 SAMPLE SOFTWARE LISTINGS

To assist the user in programming this board, a detailed sample assembly code listing for a 68000 VMEbus CPU is provided in Appendix C.

SECTION 5
CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

CAUTION

SOME OF THE COMPONENTS ASSEMBLED ON VMIC'S PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES AS SHIPPED. WHEN THE BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, ETC., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed-circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

CAUTION

DO NOT INSTALL OR REMOVE BOARDS WHILE POWER IS APPLIED.

De-energize the equipment and insert the board into an appropriate slot of the chassis, while ensuring that the card is properly aligned and oriented in the supporting card guides. Slide the card smoothly forward against the mating connector until firmly seated.

The VMIVME-DMA is compatible with any system chassis which accepts double eurocard form factor boards with front panels. The front panel provides handles for installation and captive screws to secure the board in the system chassis.

5.3 JUMPER INSTALLATION

The revision E board (and subsequent revisions of the board) also provides for jumper selection of the VMEbus priority level, board A/B selection ("Master/Slave"), GO bit control; and jumpers to enable the watchdog timer, user

forcing done, and stop burst mode. The reader should refer to Figure 5.3-1 for jumper locations.

5.3.1 VMEbus Priority Jumpers

Jumpers JE and JF provide for the selection of bus request level and grant level, respectively. The reader should refer to Figure 5.3.1-1 for selection of bus priority level (3, 2, 1, or 0). The factory configuration is level 3.

5.3.2 Board A/B Selection

Board A/B selection is factory configured as board "B" and to be under program control (see Table 5.3.2-1). However, a board may be hardwired as board A (Link Master) as shown in Table 5.3.2-1.

Table 5.3.2-1. Link Master Selection Installation of Jumper JC

BOARD SELECT A/B	JUMPER INSTALLATION
POWERS UP BOARD AS B (LINK SLAVE) CAN BE SET TO A (LINK MASTER) UNDER PROGRAM CONTROL	+5 MC PM JC
ALWAYS SELECTED AS BOARD A (LINK MASTER)	+5 MC PM JC

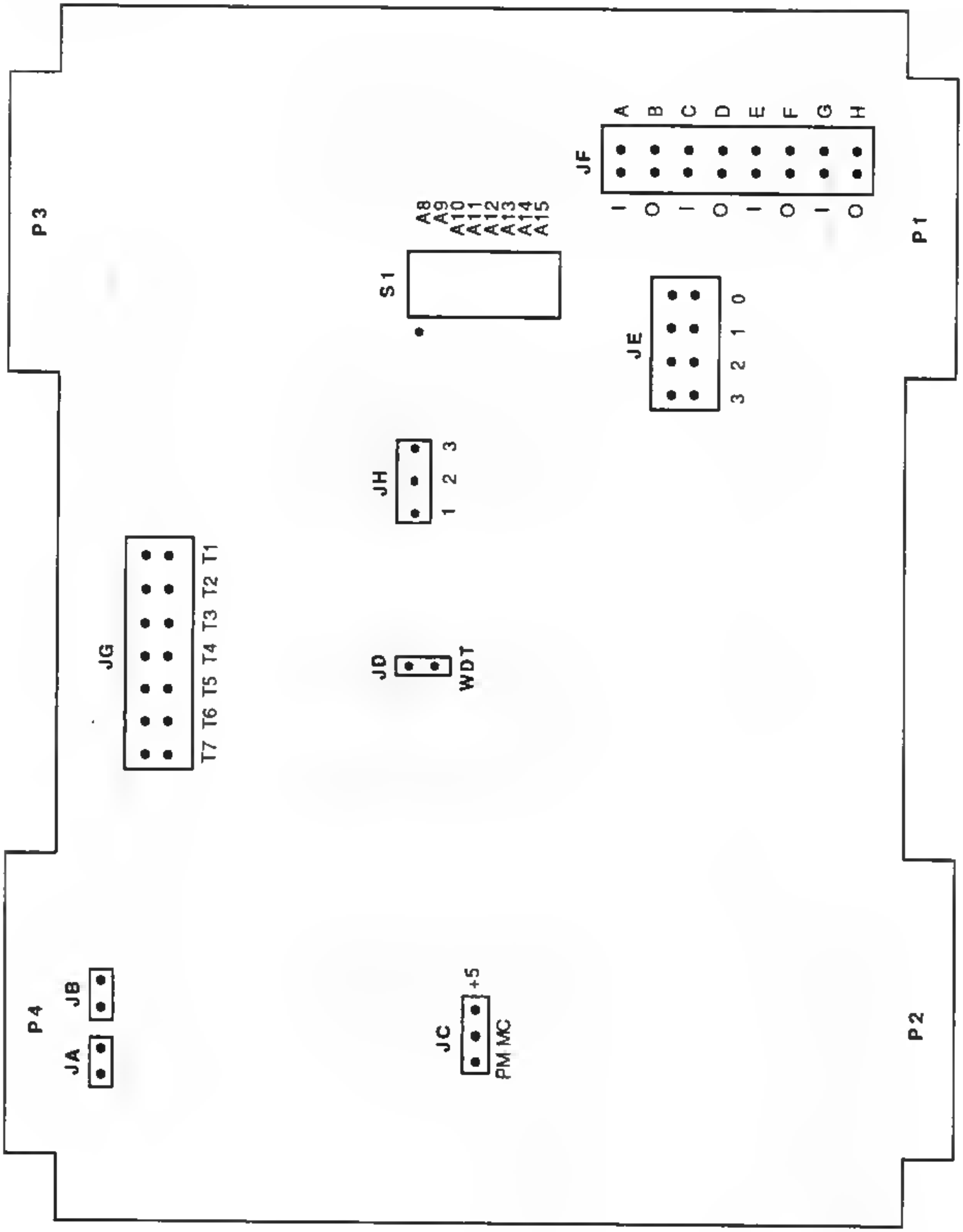
MOMA/T5.3.2-1

5.3.3 Watchdog Timer Disable

The Watchdog Timer (WDT) can be enabled by removing the WDT jumper and setting the WDT enable bit in the device Control Status Register (CSR). The factory configuration has the WDT jumper installed (see Section 4.6.2). If enabled the WDT will force a DMA DONE interrupt if no request is received over the cable for 200 milliseconds (nominal).

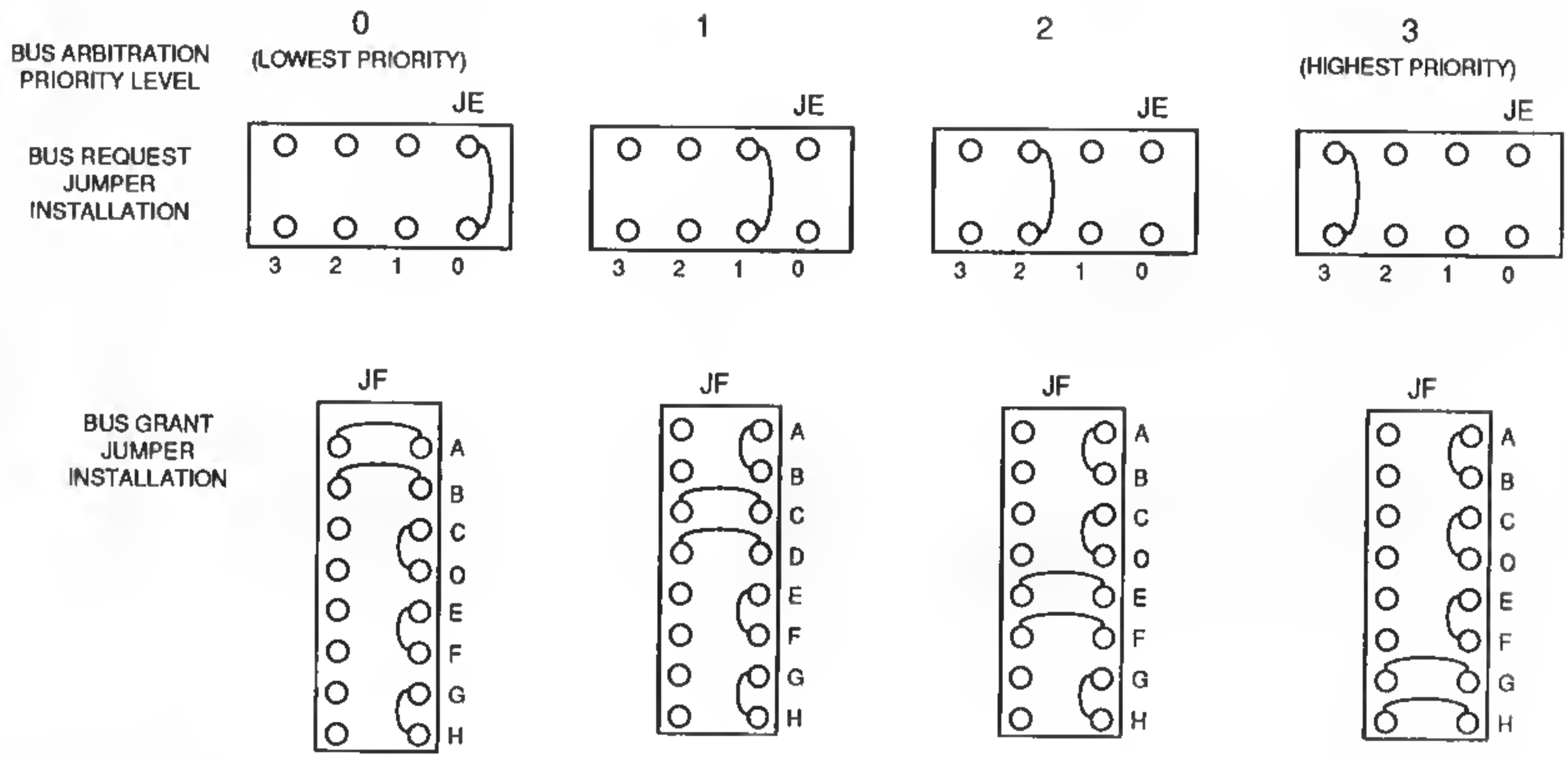
5.3.4 "User Forcing Done" and "Stop Burst" Jumpers (JA and JB)

These two jumpers should not be installed when the user is connecting two VMIVME-DMA boards back-to-back. These two jumpers should be installed only if specially designed hardware provides drivers for the two signals *USER FORCING DONE* and *STOP BURST*.



MSIU/F5.3-1

Figure 5.3-1. Switch and Jumper Locations



NOTE: This board is factory configured for level 3.

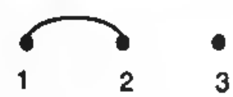
MSIU/F5.3.1-1

Figure 5.3.1-1. Jumper Installation for Selection of VMEbus Priority Level

5.3.5 Go Flip-Flop Jumper (JH)

This jumper is provided to select program control option for the GO bit (see Table 5.3.5-1).

Table 5.3.5-1. Go Flip-Flop Configuration (JH)

FUNCTION	JUMPER INSTALLATION JH
Go bit Flip-Flop cannot be cleared under program control.	
Go bit Flip-Flop can be cleared under propram control.	

MDMA/T5.3.5-1

5.3.6 Data Deskew Time Delay (Jumper JG)

Install one jumper to select time delay for data deskew (see Table 5.3.6-1). See Figure 5.3-1 for jumper locations.

5.4 BOARD BASE ADDRESS

The VMIVME-DMA occupies 256 bytes of the VMEbus short I/O space. The upper eight bits of the short address are Dual In-line Package (DIP) switch selectable. Figure 5.4-1 for selection of the board base address, and refer to Figure 5.3-1 for the location of the DIP Switch.

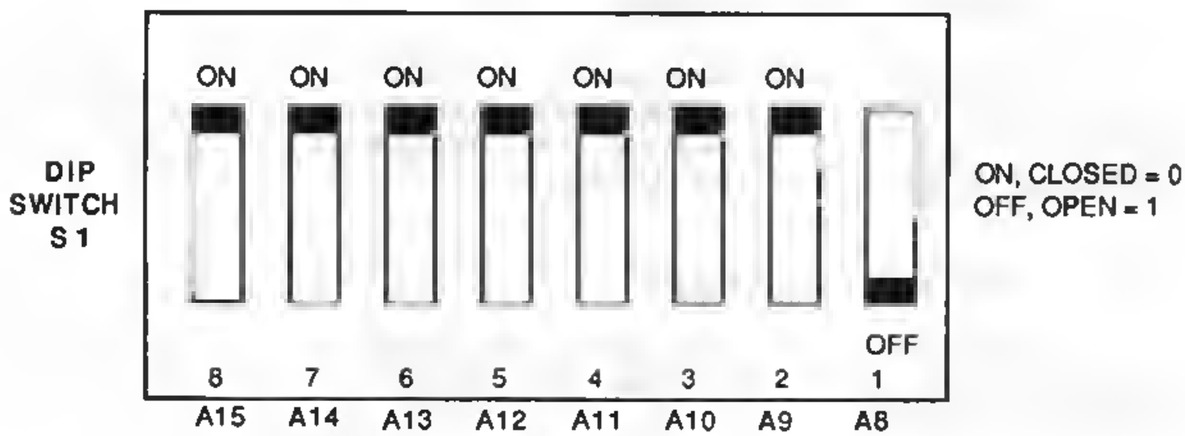
5.5 ADDRESS MODIFIERS

The board is factory configured via a programmed PAL to respond to either of two address modifier codes: short supervisory ($2D) and short non-privileged access ($29).

Table 5.3.6-1. Suggested Deskew Time Delays (Jumper Selectable at JG) vs Expected Cable Time Skew and Cable Length

JUMPER SELECTION	TIME DELAY SELECTED	CABLE LENGTH RANGES (In feet)	
		IF 10% SKEW	IF 5% SKEW
T1	62.5 ns	0 to 10 feet	0 to 20 feet
T2	125 ns	11 to 391 feet	21 to 782 feet
T3	187 ns	392 to 781 feet	783 to 1,562 feet
T4	250 ns	782 to 1,169 feet	1,563 to 2,338 feet
T5	312 ns	1,170 to 1,562 feet	2,339 to 3,124 feet
T6	375 ns	1,563 to 1,950 feet	______
T7	437 ns	1,951 to 2,344 feet	______

MDMA/T5.3.6-1



NOTE: The base address example is $0100.

Figure 5.4-1. VMIVME-DMA Base Address Configuration

5.6 I/O CABLES

The VMVIME-DMA generates a TTL bus that is terminated in 120 ohms via 180/390 ohms terminating resistors. The VMIVME-DMA may be connected to external devices or to another VMIVME-DMA, using up to 15.2 m (50-foot) cables.

I/O connector pin specifications and signal mnemonics are shown in Tables 5.6-1 and 5.6-2. The I/O connectors pin-out is designed with a high quality ground return for each signal (or data line) for increased noise immunity and high reliability. VMIC recommends the use of twisted pair cables so that the user may take advantage of this design. VMIC also recommends the use of high quality shielded cable for distances exceeding five feet. The cable shield ***MUST*** be grounded at both ends of the interface cable, if a shielded cable is used. The grounds should have low impedance at high frequencies.

For back-to-back mode, P3 should be connected to P3 on the other device and P4 should be connected to P4 on the other device, see Figure 5.6-1. The A/B jumper should be set to "A" on the one board and to "B" on the other board. Refer to Figure 5.3-1 for the location of this jumper. When connecting to a user device, the A/B jumper can either be in the A or B position. Tables 5.6-1 and 5.6-2 list the signal pinout based on the A/B jumper selection.

Table 5.6-1. Data Connector P3

PIN	ROW A SIGNAL	ROW C SIGNAL	PIN	ROW A SIGNAL	ROW C SIGNAL
1	ED00	GND	17	ED16	GND
2	ED01	GND	18	ED17	GND
3	ED02	GND	19	ED18	GND
4	ED03	GND	20	ED19	GND
5	ED04	GND	21	ED20	GND
6	ED05	GND	22	ED21	GND
7	ED06	GND	23	ED22	GND
8	ED07	GND	24	ED23	GND
9	ED08	GND	25	ED24	GND
10	ED09	GND	26	ED25	GND
11	ED10	GND	27	ED26	GND
12	ED11	GND	28	ED27	GND
13	ED12	GND	29	ED28	GND
14	ED13	GND	30	ED29	GND
15	ED14	GND	31	ED30	GND
16	ED15	GND	32	ED31	GND

MSIU/T5.6-1

Table 5.6-2. Control Connector P4

PIN	ROW A SIGNAL	ROW C SIGNAL	PIN	ROW A SIGNAL	ROW C SIGNAL
1	MASTER SPARE STATUS H	GND	17	NOT USED	GND
2	MASTER TRANSMIT CMD H	GND	18	NOT USED	GND
3	MASTER ATTN INTERRUPT H	GND	19	NOT USED	GND
4	MASTER REQUEST H	GND	20	NOT USED	GND
5	SLAVE SPARE STATUS H	GND	21	NOT USED	GND
6	SLAVE TRANSMIT CMD H	GND	22	NOT USED	GND
7	SLAVE ATTN INTERRUPT H	GND	23	NOT USED	GND
8	SLAVE REQUEST H	GND	24	NOT USED	GND
9	NOT USED	GND	25	NOT USED	GND
10	NOT USED	GND	26	NOT USED	GND
11	NOT USED	GND	27	NOT USED	GND
12	NOT USED	GND	28	NOT USED	GND
13	NOT USED	GND	29	NOT USED	GND
14	NOT USED	GND	30	NOT USED	GND
15	NOT USED	GND	31	NOT USED	GND
16	NOT USED	GND	32	NOT USED	GND

MSIU/T5.6-2

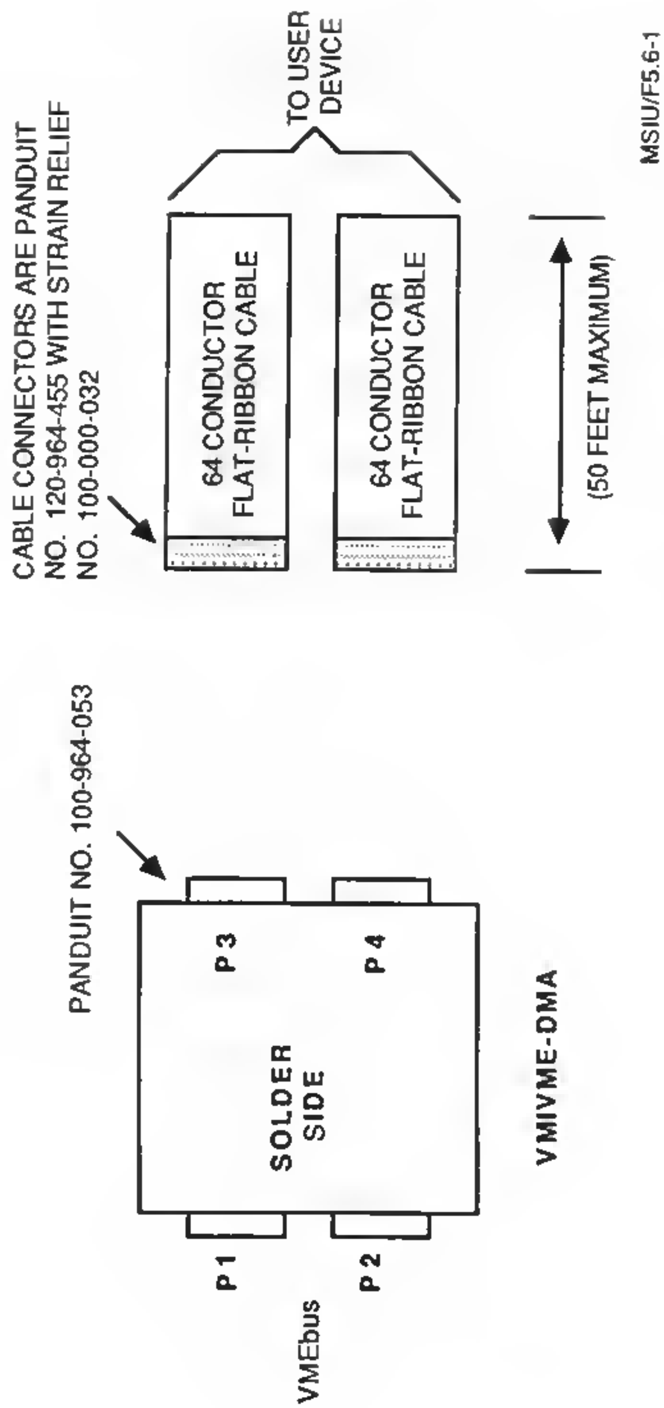


Figure 5.6-1. VMIVME-DMA Cabling Pictorial Diagram

SECTION 6

MAINTENANCE AND WARRANTY

6.1 MAINTENANCE

This section of the technical manual provides information relative to the care and maintenance of VMIC's products. Should the products malfunction, the user should verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the VMEbus card cage
h. Quality of cables and I/O connections

User level repairs are not recommended. Contact VMIC for a Return Authorization Number.

6.2 MAINTENANCE PRINTS

The appendix(ices) to this manual contain(s) drawings and diagrams for reference purposes.

6.3 WARRANTY

VMIC's Standard Products are warranted to be free from defects in material and workmanship for a period of two years (24 months) from the date of shipment. In discharge of this warranty, VMIC, at its option, agrees to either repair or replace, at VMIC's facility and at VMIC's discretion, any part, component, subassembly accessory, or any hardware, software, or system product, which under proper and normal use proves defective in material and workmanship.

The customer shall provide notice to VMIC of each such defect within a reasonable time after the customer's discovery of such defect.

In order to return the defective product(s) or part(s) at VMIC's expense, the customer must contact VMIC's Customer Service Department to obtain a Call Ticket Number. The defective product(s) or part(s) must also be properly boxed

and weighed. After a VMIC Call Ticket Number and Return Authorization Number has been obtained, the defective product(s) or part(s) may be returned (transportation collect for surface UPS) to VMIC. Any replaced or repaired product(s) or part(s) will be shipped back to the customer's at the expense of VMIC (also UPS surface).

The customer should be aware that the above process can sometimes take up to eight (8) days for the shipment to reach VMIC. The customer has the option to ship the defective product(s) or part(s) at the customer's own expense if the customer cannot afford this possible delay.

There shall be no warranty or liability on any VMIC product(s) or part(s) that is (are) damaged or subjected to accident(s), perils of nature, negligence, overtemperature, overvoltage, misapplication of electrical power, insertion or removal of boards from backplanes and/or I/O connectors with power applied by the customer(s), appointee(s), or any other person(s) without the expressed approval of VMIC.

Final determination of warranty eligibility shall be made by VMIC, and if a warranty claim is considered invalid for any reason, the customer will be charged for services performed and expenses incurred by VMIC in repair, handling and shipping the returned product or part. Determination as to whether the item is within warranty, coverage shall not be unreasonably withheld.

The warranty period of the replacement or repaired product(s) or part(s) shall terminate with the termination of the warranty period with respect to the original product(s) or part(s) for all replacement parts supplied or repairs made during the original warranty period.

THE FOREGOING WARRANTY AND REMEDY ARE EXCLUSIVE AND VMIC SHALL HAVE NO OTHER OR ADDITIONAL LIABILITY TO BUYER OR TO ANYONE CLAIMING UNDER BUYER (THIRD PARTY) UNDER ANY OTHER AGREEMENT OR WARRANTY, EXPRESS OR IMPLIED EITHER IN FACT OR BY OPERATION OF THE LAW, INCLUDING ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS, STATUTORY, OR OTHERWISE. VMIC SHALL HAVE NO LIABILITY FOR SPECIAL OR CONSEQUENTIAL DAMAGES OF ANY KIND OR FROM ANY CAUSE ARISING OUT OF THE INSTALLATION OR USE OF ANY PRODUCT FURNISHED HEREUNDER.

6.4 OUT-OF-WARRANTY REPAIR POLICY

The following sections describe VMIC's policy on repairs and warranties on repaired products.

6.4.1 Repair Category

VMIC's repair policy ot standard products is divided into two categories, depending on the item to be repaired. These categories are:

a. Product Exchange
b. Fixed Price Repair

Category 1 (product exchange) represents the tastest tum around of the two categories. In this case, the customer sends the maltunctioning product to VMIC. VMIC will return an operational product to the customer within 72 hours ot receipt provided VMIC has the product in stock. Customers should contact VMIC prior to returning products tor repair to determine stocking status.

Category 2 (Fixed Price Repair) applies to products returned to VMIC for repair and subsequent return to the customer.

Return authorizations are required on all product repairs, and all purchase orders should reter to VMIC's Return Authorization Number which is assigned by VMIC's Customer Service Department.

6.4.2 Repair Pricing

Product exchange is tifty percent (50%) ot the current list price. Fixed price repairs are performed at twenty-tive percent (25%) ot the current list price. Repair prices are not discountable.

(Repair prices are subject to change without notice).

6.4.3 Payment

Payment is due upon delivery or at VMIC's option, net thirty (30) days trom the date of delivery. Payment should be made to:

VME Microsystems International Corporation
12090 South Memorial Parkway
Huntsville, Alabama 35803-3308
Attention: Accounts Receivable

VMIC allows a one (1) percent discount tor payment made within ten (10) days of invoice date or a two (2) percent discount on payment made prior to shipment of order. This payment discount, however, does not apply to freight.

6.4.4 Shipping Charges

Shipping charges are the customer's responsibility, with the exception of warranty repairs, whereby VMIC will pay the return to customer shipping charges.

6.4.5 Shipping Instructions

The type of packaging used to ship the product depends on whether the product is shipped singly, in a chassis, or packaged with other boards. The shipper should carefully pack the product(s), using the same precautions listed in the "unpacking procedures". The user should utilize the same (or equivalent) protective packaging container for re-shipment as provided by VMIC. Approved ESD procedures are recommended when handling VMIC's products.

6.4.6 Warranty on Repairs

Products repaired by VMIC are warranted against defects in workmanship and material for a period of ninety (90) days from date of shipment to the customer for all products that were repaired out of warranty. See Standard Conditions of Sale for products repaired within the warranty.

6.4.7 Exclusions

Repair rates may not apply to products which have received unusual physical or electrical damage. In such cases, VMIC will provide an estimated price for product repair or replacement. The customer may then choose to have the product repaired at the estimated price, returned unrepaired at no charge, or replaced at VMIC's current list price.

APPENDIX A

ASSEMBLY DRAWING, PARTS LIST, AND SCHEMATIC

REVISIONS

132 REV.	332 REV.	DESCRIPTION	BY	DATE	APPR.
B	B	E.C.O. 88-0029 TECHNICAL REVIEW ADD ASSEMBLY DRAWING	S. Wortz	5/2/88	M. LEMLEY
C	C	E.C.O. 88-0137 MINOR CORRECTIONS	S. Wortz	6/21/88	M. LEMLEY
D	D	E.C.O. 89-0055 ADD REWORK INSTRUCTIONS, ADD CORRECTIONS	D. O'TOOLE	7/12/89	T. THORNTON
E	E	E.C.O. 89-0146	D. SMITH	10/25/89	T. THORNTON
F	E	CHANGES PER ECO 89-0175	D. O'TOOLE	1/12/90	T. THORNTON
G	E	CHANGES PER ECO 90-0072	E.M.GREEN	6/1/90	T. THORNTON
H	F	CHANGES PER ECO 90-0196	E.M.GREEN	11/29/90	T.L.T.

NOTES:

1. FOR SCHEMATIC DIAGRAM SEE 141-000DMA-000
2. FOR TEST PROCEDURE SEE S10-000DMA-000

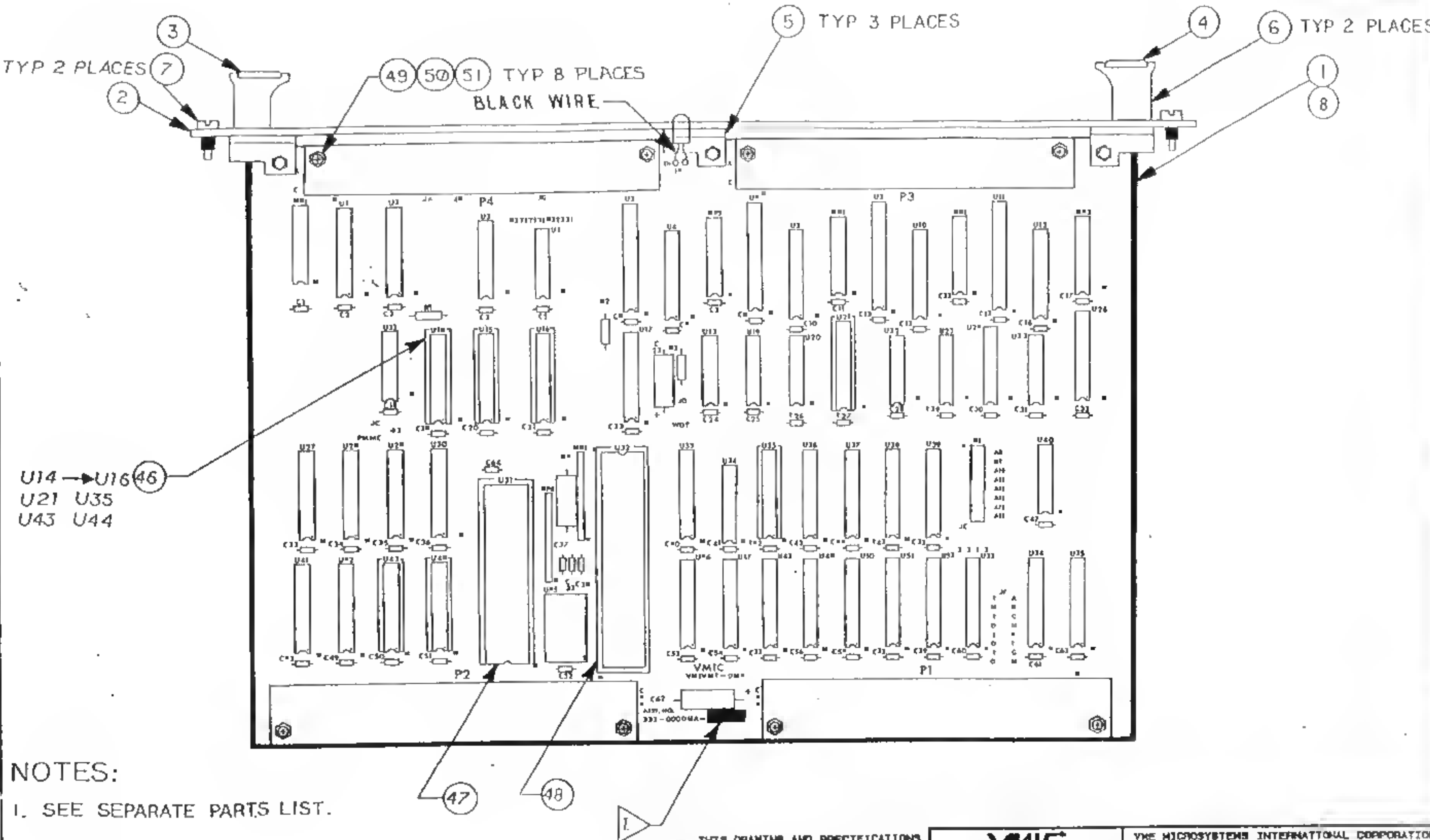
REV	H	E	G	G	F	G	G	D	REVISION STATUS OF SHEETS
SHT	1	2	3	4	5	6	7	8	

APPROVALS		DATE
DRAWN	S. Lemley	5/4/88
PROJ. ENG.	M. LEMLEY	5/4/88
ENG. MGR.	P. RAINOSEK	5/4/88
PROD.	D. FOWLER	5/4/88
Q.A.	S. KEAGLE	5/4/88

VMIC
12090 SO. MEM. PKWY.
HUNTSVILLE, AL. 35803
VME MICROSYSTEMS INTERNATIONAL CORPORATION

ASSEMBLY DRAWING
VMIVME-DMA

SIZE		DWG NO.	REV.
A	0BPH5	132-000DMA-000	H
SCALE			SHEET 1



NOTES:

1. SEE SEPARATE PARTS LIST.

VMIC		VME MICROSYSTEMS INTERNATIONAL CORPORATION 12090 SOUTH MEMORIAL PARKWAY HUNTSVILLE, ALABAMA 35803-3308		
SIGNATURES	DATE	SIZE B	OBPH5	DWG NO 132-000MA-0 REV E
DRAWN J. E. O'Neal	6-8-89			
CHECKED R. Freeland	10-24-89	SCALE 1TO1		SHEET 2

PARTS LIST

VMIC VME MICROSYSTEMS INT'L CORP.			CODE IDENT. NO.	DWG. NO. 132-000DMA-000	REV. LTR. G
MODEL NO. UMIUME-DMA		SIGNATURE	DATE	CONTRACT NO.	SH 3
	DRAWN		5/2/88		
	CHECKED	S.E. O'Neal	11-15-90		

INSTRUCTIONS:

L **NOTES:**

A. ALL ASSEMBLED BOARDS SHALL BE IDENTIFIED WITH THE ASSEMBLED BOARD PART NUMBER. THIS NUMBER INCLUDES THE CURRENT REVISION LETTER LISTED IN THE 332-COLUMN OF THE REVISION TABLE, FOUND ON SHEET ONE. THE RESULTING PART SHALL BECOME A 332-000DMA-000 (REV.)

B. THE REVISION LETTER(S) OF THE ASSEMBLY DRAWING SHALL BE STAMPED IN THE DESIGNATED AREA.

C. REMOVE THE EXISTING REVISION LETTER FROM THE 332 ASSEMBLED PART NUMBER.

D. REMOVABLE, NON-SMEARING INK SHALL BE USED TO STAMP REVISION LETTERS IN THE DESIGNATED AREA.

PARTS LIST

VMIC VME MICROSYSTEMS INT'L CORP.	CODE IDENT. NO.	DWG. NO. 132-000DMA-000	REV. LTR. G
MODEL NO. UMIVME-DMA	SIGNATURES / DATE: DRAWN D. O'TOOLE 5/25/89; CHECKED S. E. O'Neil 11-15-90	CONTRACT NO.	SH 30

INSTRUCTIONS: REWORK

NOTES:

A. REWORK INSTRUCTIONS SHALL BE ACCOMPLISHED ON THE COPPER REVISION(S) INDICATED AND WILL BECOME A PART OF THE ASSEMBLED BOARD.

B. REWORK INSTRUCTION SYMBOLS

1. ■ PIN ONE DOT
2. ● DRILL HOLE
3. >< DISCONNECT TRACE
4. ---- TRACE ON INTERNAL LAYER
5. —— TRACE ON EXTERNAL LAYER

PARTS LIST

VMIC VME MICROSYSTEMS INT'L CORP.		CODE IDENT. NO.	DWG. NO. 132-000DMA-000	REV. LTR. G
MODEL NO. UMIVME-DMA	SIGNATURE: DRAWN S. Wong / CHECKED S. E. O'Neal	DATE: 5/2/88 / 11-15-90	CONTRACT NO.	SH 38

EFFECTIVITY: E.C.O. DMA-09
REV. D COPPER
(FC-01)

INSTRUCTIONS: REWORK

STEP 1
CUT U20 PIN 12 FROM U20 PIN 14 (+5 ON SOLDER SIDE).

STEP 2
CONNECT U20 PIN 12 TO GROUND.

STEP 3
CUT U1 PIN 1 FROM GROUND (SOLDER SIDE).

STEP 4
CUT U2 PIN 1 FROM GROUND (SOLDER SIDE).

STEP 5
CONNECT U1 PIN 1 TO +5V.

STEP 6
CONNECT U2 PIN 1 TO +5V.

STEP 7
CONNECT U32 PIN 15 TO U14 PIN 1.

PARTS LIST

VMIC VME MICROSYSTEMS INT'L CORP.			CODE IDENT. NO.	DWG. NO. 132-000DMA-000	REV. LTR. G
MODEL NO. UMIVME-DMA	SIGNATURE	DATE	CONTRACT NO.		SH 3C
	DRAWN S.Wagz	5/2/88			
	CHECKED S.E. O'Neal	11-12-90			

EFFECTIVITY: E.C.O. 88-0029 E.C.O. 89-0055
REV. D, F, & G COPPER

INSTRUCTIONS: REWORK

STEP 1

CHANGE PAL 5 (U43) FROM N/R TO PAL E (U43) REV. A.
P/N: 303-000132-000
FILE/NUM: 163-000132-000
FILE NAME: DMAV43A.PS

PARTS LIST

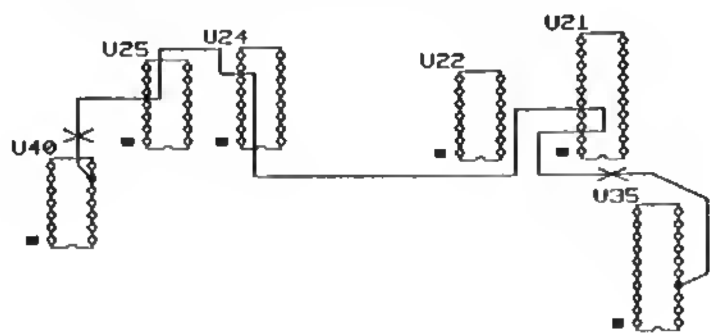
VMIC™ VME MICROSYSTEMS INT'L CORP.	CODE IDENT. NO.	DWG. NO. 132-0000MA-000	REV. LTR. G
MODEL NO. VMIVME-DMA	SIGNATURES: DRAWN D. O'TOOLE, DATE 5/25/89; CHECKED (signature), DATE 11-15-90	CONTRACT NO.	SN 3D

EFFECTIVITY: E.C.O. 89-0055
REV. D, F, & G COPPER

INSTRUCTIONS: REWORK

STEP 1 (SOLDER SIDE)

CUT U35/PIN 17 FROM U40/PIN 9.



STEP 2

CONNECT U35/PIN 17 TO U14/PIN 14.

PARTS LIST

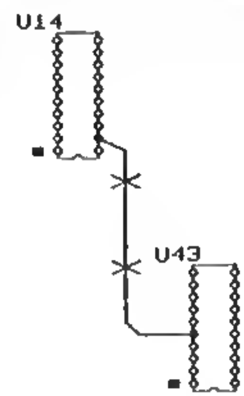
VMIC VME MICROSYSTEMS INT'L CORP.		CODE IDENT. NO.	DWG. NO. 132-000DMA-000	REV. LTR. G
MODEL NO. UMIUME-DMA	SIGNATURES	DATE	CONTRACT NO.	SN 3E
	DRAWN D. O'TOOLE	5/25/89		
	CHECKED R. E. O'Neal	11-15-90		

EFFECTIVITY: E.C.O. 89-0055
REV. D, F, & G COPPER

INSTRUCTIONS: REWORK (CONTINUED)

STEP 3 (SOLDER SIDE)

CUT U14/PIN 19 FROM U43/PIN 5.



STEP 4

CONNECT U14/PIN 15 TO U43/PIN 5.

STEP 5

CONNECT U14/PIN 16 TO U40/PIN 9.

PARTS LIST

VMIC VME MICROSYSTEMS INT'L CORP.	CODE IDENT. NO.	DWG. NO. 132-000DMA-000	REV. LTR. G
MODEL NO. VMIVME-DMA	SIGNATURES / DATE DRAWN D. O'TOOLE 5/25/89 CHECKED S. E. O'Neil 11-15-90	CONTRACT NO.	SN 3F

EFFECTIVITY: E.C.O. 89-0055
REV. D, F, & G COPPER

INSTRUCTIONS: REWORK (CONTINUED)

STEP 6

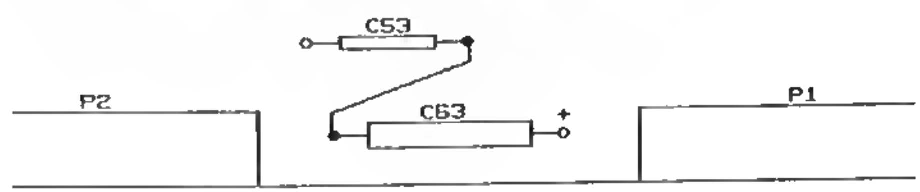
CHANGE PAL A (U35) FROM N/R TO PAL A (U35) REV. A.
P/N: 303-000128-000
FILE NUM.: 163-000128-000
FILE NAME: DMAU35A.PS

STEP 7

CHANGE PAL G (U14) FROM N/R TO PAL G (U14) REV. A.
P/N: 303-000134-000
FILE NUM.: 163-000134-000
FILE NAME: DMAU14A.PS

STEP 8

CONNECT GROUND SIDE OF C63 TO GROUND SIDE OF C53
(COMPONENT SIDE) USING 24 GAUGE WIRE.



PARTS LIST

VMIC VME MICROSYSTEMS INT'L CORP.		CODE IDENT. NO.	DWG. NO. 132-000DMA-000	REV. LTR. G
MODEL NO. UMIUME-DMA	SIGNATURES: DRAWN D. SMITH; CHECKED G. E. O'Neal	DATE: 10/17/89; 11-15-90	CONTRACT NO.	SH 3G

EFFECTIVITY: E.C.O. 89-0146
REV. F & G COPPER

INSTRUCTIONS: REWORK (CONTINUED)

STEP 1 (COMPONENT SIDE):

CUT TRACE FROM U13-3 TO U17-18 AT U13-3.

STEP 2:

CONNECT U13-3 TO U17-9 (SOLDER SIDE).

STEP 3 (SOLDER SIDE):

CUT TRACE FROM U13-1 TO U14-4 AT U13-1.

STEP 4

CONNECT U13-1 TO U14-17.

STEP 5

CHANGE PAL G (U14) REV. A TO PAL G (U14) REV. A
CHANGE P/N: 303-000134-000 TO P/N: 303-000294-000
CHANGE FILE NAME: DMAU14A.PLD TO DMAU14B.PLD

PARTS LIST

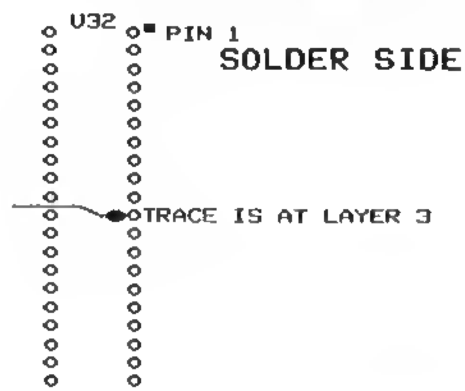
VMIC — VME MICROSYSTEMS INT'L CORP.		CODE IDENT. NO.	DWG. NO. 132-000DMA-000	REV. LTR. G
MODEL NO. UMIVME-DMA	SIGNATURES / DATE: DRAWN E.M.GREEN 11/13/90; CHECKED S.E. O'Neal 11-21-90		CONTRACT NO.	SN 3H

EFFECTIVITY: E.C.O. 90-0196
REV. F & G COPPER

INSTRUCTIONS: REWORK

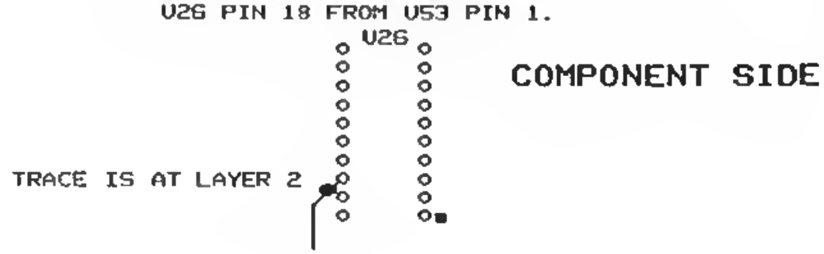
STEP 1

DRILL FROM SOLDER SIDE AT U32 PIN 11 TO DISCONNECT U32 PIN 11 FROM U48 PIN 9.



STEP 2

DRILL FROM COMPONENT SIDE AT U26 PIN 18 TO DISCONNECT U26 PIN 18 FROM U53 PIN 1.



PARTS LIST

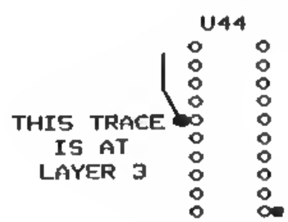
VMIC VME MICROSYSTEMS INT'L CORP.			CODE IDENT. NO.	DWG. NO. 132-080DMA-008	REV. LTR. G
MODEL NO. UMIUME-DMA	SIGNATURES	DATE	CONTRACT NO.		SH 31
	DRAWN E.M.GREEN	11/13/90			
	CHECKED D.E. O'Neil	11-15-90			

EFFECTIVITY: E.C.O. 90-0196
REV. F & G COPPER

INSTRUCTIONS: REWORK

STEP 3

DRILL FROM COMPONENT SIDE AT U44 PIN 15 TO DISCONNECT U26 PIN 18 FROM U44 PIN 15.



STEP 4

CONNECT U14 PIN 1 TO U15 PIN 7

STEP 5

CONNECT U48 PIN 9 TO U15 PIN 8

STEP 6

CONNECT U15 PIN 19 TO U32 PIN 11

STEP 7

CONNECT U15 PIN 14 TO U26 PIN 18

STEP 8

CONNECT U53 PIN 19 TO U44 PIN 15

STEP 9

REMOVE PAL FROM U15 AND INSERT PAL C FILE NAME: DMAU15B.PLD,
PART# 303-000453-000.

END OF REWORK INSTRUCTIONS

PARTS LIST

VMIC

VME MICROSYSTEMS INT'L CORP.

CODE IDENT. NO.	DWG. NO.	REV. LTR.
	132-000DMA-000	G

MODEL NO.	SIGNATURES	DATE	CONTRACT NO.	
UMIUME-DMA	DRAWN [signature]	5/2/80		SH 4
	CHECKED O. JESSEE	5/23/90		

QUANTITY REQ'D SUB-ASSEMBLY	ITEM NO.	REF. DES.	PART NO. OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	STD. PART NO. / SPEC. DWG. NO.
1	1		333-00DMA0-000	BOARD: PC, RAW, 6 LAYERS	
1	2		324-000000-000	FRONT PANEL: TWO MIDDLE 64 PIN CONNECTOR, CENTER MOUNT FAIL LED	151-0000008-00
1	3		324-000000-001	LOGO: ASSEMBLED-VMIC, SINGLE	151-000000-001
1	4		324-999907-000	LOGO: ASSEMBLED-DMA, SINGLE	151-999987-000
1.5	5	HARD-WARE	324-900000-001	KIT: MOUNTING, FRONT PANEL	VERO BICC 173-12525B
2	6	HARD-WARE	324-900003-000	HANDLE: FRONT PANEL	VERO BICC 172-38201F
1	7	HARD-WARE	328-25051S-000	SCREW KIT: FRONT PANEL	VERO BICC 172-22729C
A/R	8	HARD-WARE	SN60	SOLDER 60\40	
6	9	U1,U2 U6,U8 U10,U12	331-304645-200	IC: DIGITAL, OCTAL BUS TRANSCEIVER, PLASTIC DIP	74AS645
1	10	U3	331-304175-600	IC: DIGITAL, QUAD D TYPE FLIP FLOP W/CLEAR, PLASTIC DIP	74LS175
1	11	U4	331-304164-600	IC: DIGITAL, 8 BIT SNIFT REGISTER, PLASTIC DIP	74LS164
4	12	U5,U7 U9,U11	331-309024-100	IC: MICROPROCESSOR, OCTAL BIDIRECTIONAL BUS LATCH, PLASTIC DIP	AMD AM2952DC
1	13	U13	331-300438-600	IC: DIGITAL, QUAD 2-INPUT NAND BUFFER, PLASTIC DIP	74LS38
3	14	U17,U26 U47	331-304641-110	IC: DIGITAL, OCTAL BUS TRANSCEIVER, PLASTIC DIP	74ALS641-1

PARTS LIST

VMIC

VME MICROSYSTEMS INT'L CORP.

CODE IDENT. NO.	DWG. NO.	REV. LTR.
	132-000DMA-000	F

MODEL NO.	SIGNATURES	DATE	CONTRACT NO.	
VMIVME-DMA	DRAWN [signature]	5/2/88		SH 5
	CHECKED D. JESSEE	5/30/90		

QUANTITY REQ'D SUB-ASSEMBLY	ITEM NO.	REF. DES.	PART NO. OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	STD. PART NO. / SPEC. DWG. NO.
3	15	U18, U19 U20	331-300474-600	IC: DIGITAL, DUAL D FLIP FLOP, PLASTIC DIP	74LS74
1	16	U22	331-304164-400	IC: DIGITAL, 8 BIT GATED SERIAL-IN, PARALLEL-OUT, FAST, PLASTIC DIP	74F164
1	17	U23	331-300474-100	IC: DIGITAL, DUAL D FLIP FLOP, PLASTIC DIP	74ALS74
1	18	U24	331-300431-600	IC: DIGITAL, DELAY ELEMENT, PLASTIC DIP	74LS31
1	19	U25	331-300432-100	IC: DIGITAL, QUAD 2-INPUT OR GATE, PLASTIC DIP	74ALS32
5	20	U27, U29 U38, U53 U48	331-304244-100	IC: DIGITAL, OCTAL BUFFER/LINE DRIVER, PLASTIC DIP	74ALS244
2	21	U28, U30	331-304273-600	IC: DIGITAL, OCTAL D FLIP FLOP, PLASTIC DIP	74LS273
1	22	U31	331-309034-012	IC: DIGITAL, HEX CONTACT BOUNCE ELIMINATOR, PLASTIC DIP	MOTOROLA MC68153
1	23	U32	331-309000-122	IC: MICROPROCESSOR, 12.5 MHZ, DIRECT MEMORY ACCESS INTERFACE, PLASTIC DIP	MOTOROLA SCB68430
2	24	U33, U46	331-304245-600	IC: DIGITAL, OCTAL BUS TRANSCEIVER, PLASTIC DIP	74LS245
1	25	U34	331-304138-100	IC: DIGITAL, 1 TO 8 DECODER/ DEMULTIPLEXER, PLASTIC DIP	74ALS138
2	26	U36, U37	331-304374-600	IC: DIGITAL, OCTAL D FLIP FLOP, W/TRI STATE OUTPUTS, PLASTIC DIP	74LS374
1	27	U39	331-304520-100	IC: DIGITAL, 8 BIT IDENTITY COMPARATOR, PLASTIC DIP	74ALS520
1	28	U40	331-300432-200	IC: DIGITAL, QUAD 2-INPUT OR GATE, PLASTIC DIP	74AS32

PARTS LIST

VMIC			
VME MICROSYSTEMS INT'L CORP.	CODE IDENT. NO.	DWG. NO. 132-000DMA-000	REV. LTR. G
MODEL NO. UMIUME-DMA	SIGNATURES: DRAWN — DATE 5/2/88; CHECKED — DATE 11/26/90	CONTRACT NO.	SN 6

QUANTITY REQ'D SUB-ASSEMBLY	ITEM NO.	REF. DES.	PART NO. OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	STD. PART NO. / SPEC. DWG. NO.
8	29	U41,U42 U49→U52 U54,U55	331-304645-110	IC: DIGITAL, OCTAL BUS TRANSCEIVER, PLASTIC DIP	74ALS645-1
1	30	U45	323-000000-120	CRYSTAL: 12 MNZ, 5V, 50/50 SYMETRY, ±100PPM FREQUENCY STABILITY, 0 TO 70°C	MOTOROLA RASCO-1 12.0 MHZ
61	31	C1 → C22 C24 → C36 C40 → C62	315-205002-104	CAP: .1 µF, .300 LEAD SPACE, 20%, 50V, Z5U, CERAMIC MONOLYTHIC	SPRAGUE 923CZ5U104M050B
		C37,C38 C39,C64			
2	32	C23,C63	315-902000-476	CAP: 47 µF, AXIAL, 20%, 35V, ALUMINUM ELECTROLYTIC	PANASONIC ECEB1VU470
5	33	RP1 → RP5	347-00110S-001	DIP: 180/390 Ω, 16 PIN, DUAL TERMINATOR, 181/391	BOURNS 4116R-003-181/391
1	34	RP6	347-001002-472	SIP: 4.7K Ω, BUSSED, 10 PIN, LOW PROFILE	BOURNS 4610X-101-472
2	35	R1,R2	347-000000-110	RESISTOR: 110 Ω, 1/4W, 5%, CARBON FILM	
1	36	R3	347-000000-103	RESISTOR: 10K Ω, 1/4W, 5%, CARBON FILM	
1	37	R4	347-000000-160	RESISTOR: 16 Ω, 1W, 5%, CARBON FILM	
55	38	JA,JB JC,JD JE,JF JG,JH	321-000016-011	TERMINAL: PC BOARD, SINGLE ROW, .025 THICK, .310 LEAD LENGTN, ONE POST	PANDUIT 92983401-01
26	39	JA,JD JC,JD JE,JF JG,1,2,3	321-00001S-001	JUMPER: PC BOARD, 2 POSITION, FEMALE, UNPLATED CONTACT, BLACK	McKENZIE MSB-2360-T-C-STP

PARTS LIST

VMIC
UME MICROSYSTEMS INT'L CORP.

CODE IDENT. NO.	DWG. NO.	REV. LTR.
	132-000DMA-000	G

MODEL NO. UMIUME-DMA

SIGNATURES		DATE
DRAWN	S.Wong	5/2/80
CHECKED	D. JESSEE	5/30/80

CONTRACT NO.

SN 7

QUANTITY REQ'D SUB-ASSEMBLY	ITEM NO.	REF. DES.	PART NO. OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	STD. PART NO. / SPEC. DWG. NO.
1	40	D1	337-000001-110	DIODE: LED, RED, 5V, 15mA, INTEGRAL RESISTOR, WIRE LEADS	DIALIGHT 558-0102-003
1	41	U14	303-000294-000	PAL G, FILE: DMAU14B.PLD, A PROGRAMMED 16L8A	331-300100-100
1	42	RP7	347-001002-222	SIP: 2.2K Ω, BUSSED, 10 PIN, LOW PROFILE	BOURNS 4610X-101-222
1	43	S1	351-000000-080	SWITCH: DIP, 8 POSITION, LOW PROFILE, PC MOUNT, TAPE SEAL	AUGAT ADF-08PCT
2	44	P1,P2	321-000011-300	CONNECTOR: DIN, 96 PIN, WAVE SOLDER, ANGLED, TYPE C, MALE	PANDUIT 100-096-053
2	45	P3,P4	321-000013-105	CONNECTOR: FLAT CABLE, 64 PIN, .114 ANGLED, WITH EJECTOR LATCHES, TYPE C, MALE	PANDUIT 120-964-053A
7	46	U14,U15 U16,U21	321-001320-001	SOCKET: DIP, 20 PIN, .300 ROW	SAMTEC ICA-320-SGT
		U35,U43 U44			
1	47	U31	321-001640-001	SOCKET: DIP 40 PIN, .600 ROW	SAMTEC ICA-640-SGT
1	40	U32	321-001640-001	SOCKET: DIP 40 PIN, .600 ROW	SAMTEC ICA-648-SGT
0	49	P1,P2 P3,P4	328-250000-010	SCREW: METRIC, 2.5 X 10MM, SS	
8	50	P1,P2 P3,P4	328-250001-025	NUT: METRIC. 2.5MM, HEX, SS	
A/R	51			LOCTITE	
1	52	U44	303-000129-000	PAL B, FILE: DMAU44A.PLD, A PROGRAMMED 16L8A	331-300100-100

PARTS LIST

QUANTITY REQ'D	VMIC	CODE IDENT. NO.	DWG. NO.	REV. LTR.
	VME MICROSYSTEMS INT'L CORP.		132-000DMA-000	D
	MODEL NO. UMIVME-DMA	SIGNATURES: DRAWN D. O'TOOLE, DATE 5/25/89; CHECKED G.E. O'Neal, DATE 11-15-90	CONTRACT NO.	SH 8 OF 8

SUB-ASSEMBLY	ITEM NO.	REF. DES.	PART NO. OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	STD. PART NO. / SPEC. DWG. NO.
1	53	U15	303-000453-000	PAL C. FILE: DMAU15B.PLD. A PROGRAMMED 16L8A	331-300100-100
1	54	U16	303-000133-000	PAL F. FILE: DMAU16A.PLD. A PROGRAMMED 16L8A	331-300100-100
1	55	U21	303-000131-000	PAL D. FILE: DMAU21A.PLD. A PROGRAMMED 16L8A	331-300100-100
1	56	U35	303-000128-000	PAL A, FILE: DMAU35A.PLD. A PROGRAMMED 16L8B	331-300100-200
1	57	U43	303-000132-000	PAL E. FILE: DMAU43A.PLD. A PROGRAMMED 16L8A	331-300100-100

NOTES:

PAL LOCATION CHART

PAL	'U' NUMBER	PAGE NUMBER
A	U35	4.5.14
B	U44	5
C	U15	9
D	U21	7
E	U43	10-11-15
F	U16	11
G	U14	14

REVISIONS

REV.	DESCRIPTION	BY	DATE	APPR.
G	E.C.O. 88-0029	[illegible]	5/12/88	M. LEMLEY
H	E.C.O. 89-0055	D. O'TOOLE	7/19/89	T. THORNTON
J	E.C.O. 89-0175	D. O'TOOLE	1/12/90	T. THORNTON
K	E.C.O. 90-0196	E.M.GREEN	11/29/90	T.L.T.
L	E.C.O. 90-0219	E.M.GREEN	2/11/91	T.L.T.

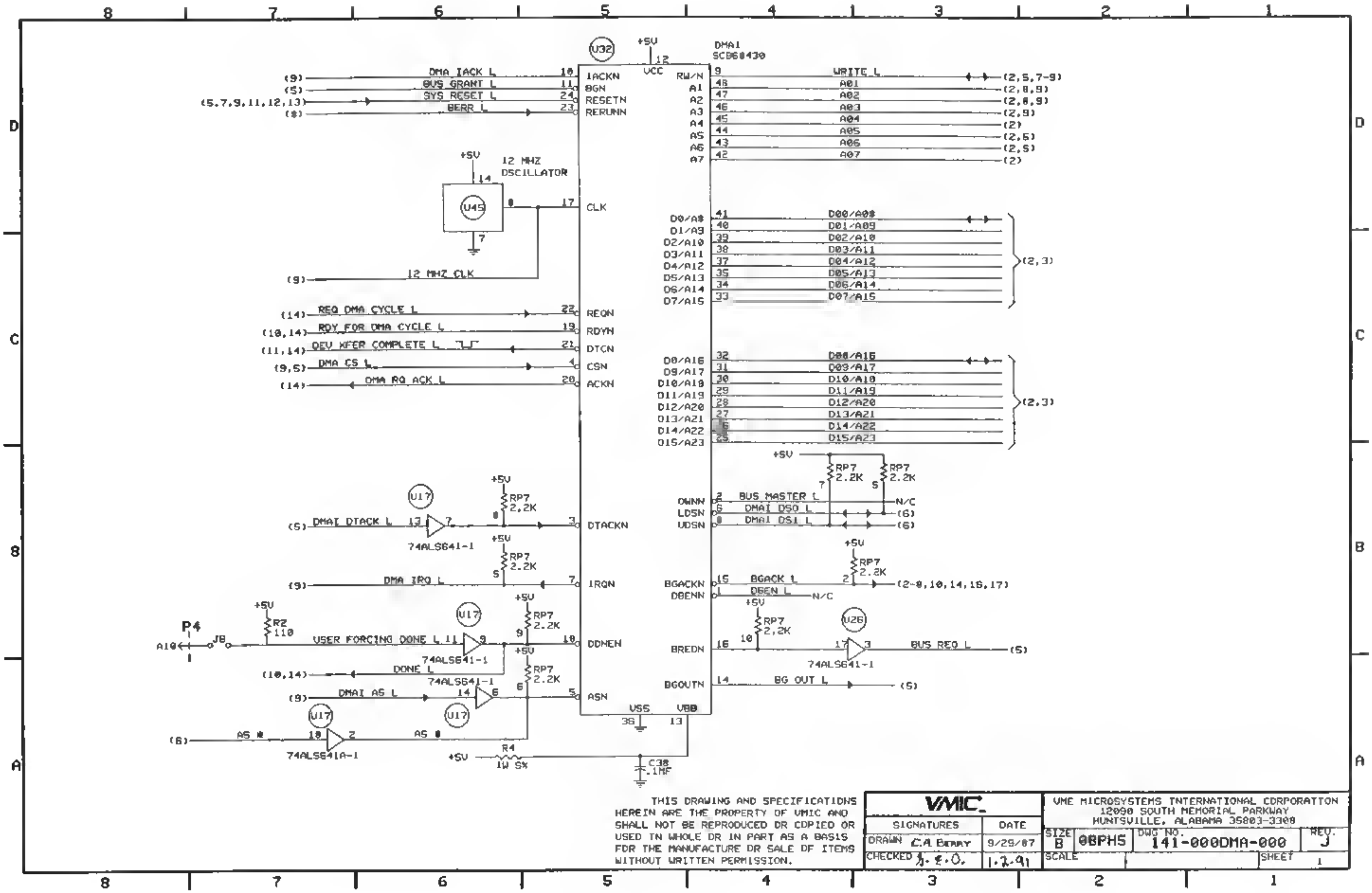
REV	L	J	J	J	J	K	K	J	J	J	J	K	J	J	J	K	J	J	REVISION STATUS OF SHEETS
SHT	A1	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

SIGNATURES		DATE
DRAWN	C.A. Berry	10/9/87
PROJ. ENG.	M. LEMLEY	2/15/88
ENG. MGR.	S.L. MAY	7/24/89
PROD.	D. FOWLER	7/24/89
Q.A.	C. MUZZEY	2/15/88

VMIC
VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SO. MEM. PKWY.
HUNTSVILLE, AL. 35803-3308

UMIVME- DMA

SIZE		DWG NO.	REV.
B	0BPH5	141-000DMA-000	L
SCALE		SHEET	A1


DMA1
SCB68430
U32
IACKN
BGN
RESETN
RERUNN
CLK
REQN
RDYN
DTCN
CSN
ACKN
DTACKN
IRQN
DDNEN
ASN
VCC
VSS
VBB
RW/N
A1
A2
A3
A4
A5
A6
A7
D0/A8
D1/A9
D2/A10
D3/A11
D4/A12
D5/A13
D6/A14
D7/A15
D8/A16
D9/A17
D10/A18
D11/A19
D12/A20
D13/A21
D14/A22
D15/A23
OWNN
LDSN
UDSN
BGACKN
DBENN
BREDN
BGOUTN
DMA IACK L
BUS GRANT L
SYS RESET L
BERR L
12 MHZ OSCILLATOR
U45
12 MHZ CLK
REQ DMA CYCLE L
RDY FOR DMA CYCLE L
DEV XFER COMPLETE L
DMA CS L
DMA RQ ACK L
DMAI DTACK L
DMA IRQ L
USER FORCING DONE L
DONE L
DMAI AS L
AS
P4
A10
J8
RZ
110
R4
1W 5%
C38
.1MF
WRITE L
A01
A02
A03
A04
A05
A06
A07
D00/A08
D01/A09
D02/A10
D03/A11
D04/A12
D05/A13
D06/A14
D07/A15
D08/A16
D09/A17
D10/A18
D11/A19
D12/A20
D13/A21
D14/A22
D15/A23
BUS MASTER L
DMAI DS0 L
DMAI DS1 L
BGACK L
DBEN L
BUS REQ L
BG OUT L
N/C
RP7
2.2K
+5V
U17
U26
74ALS641-1
74ALS641A-1
(2,5,7-9)
(2,8,9)
(2,9)
(2,5)
(2)
(2,3)
(2-8,10,14,16,17)
(5,7,9,11,12,13)
(10,14)
(11,14)
(9,5)
(14)
(9)
(5)
(6)
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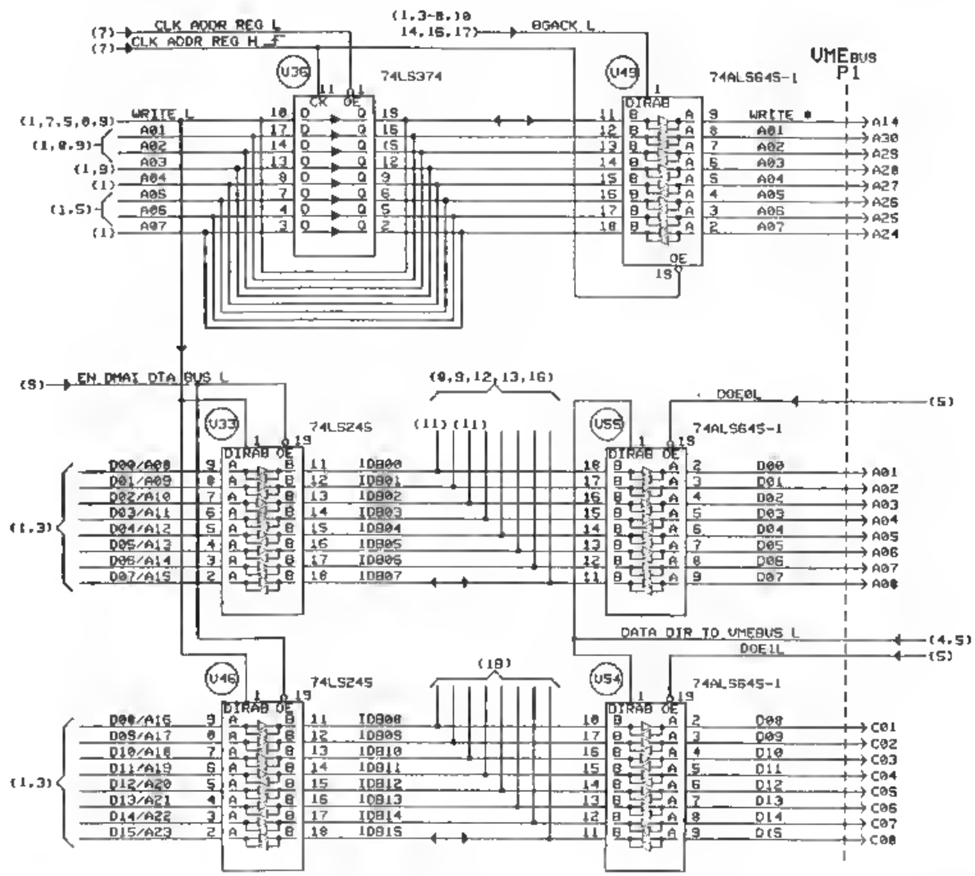
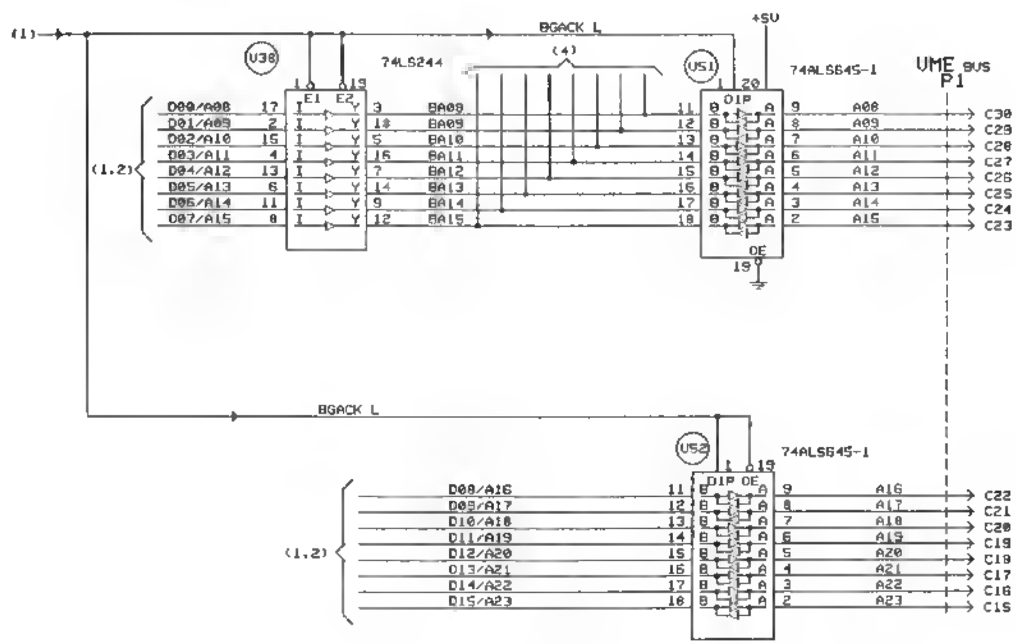
VMIC
SIGNATURES
DATE
DRAWN C.A. Berry
9/29/87
CHECKED
1.2.91
VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308
SIZE B
08PH5
DWG NO. 141-000DMA-000
REV. J
SCALE
SHEET 1



VMIC		VME MICROSYSTEMS INTERNATIONAL CORPORATION 12090 SOUTH MEMORIAL PARKWAY HUNTSVILLE, ALABAMA 35803-3308			
SIGNATURES	DATE	SIZE		DWG NO.	REV.
DRAWN C.A Berry	9/29/87	B	0BPH5	141-000DMA-000	J
CHECKED S.R.O.	1-2-90	SCALE		SHEET	2

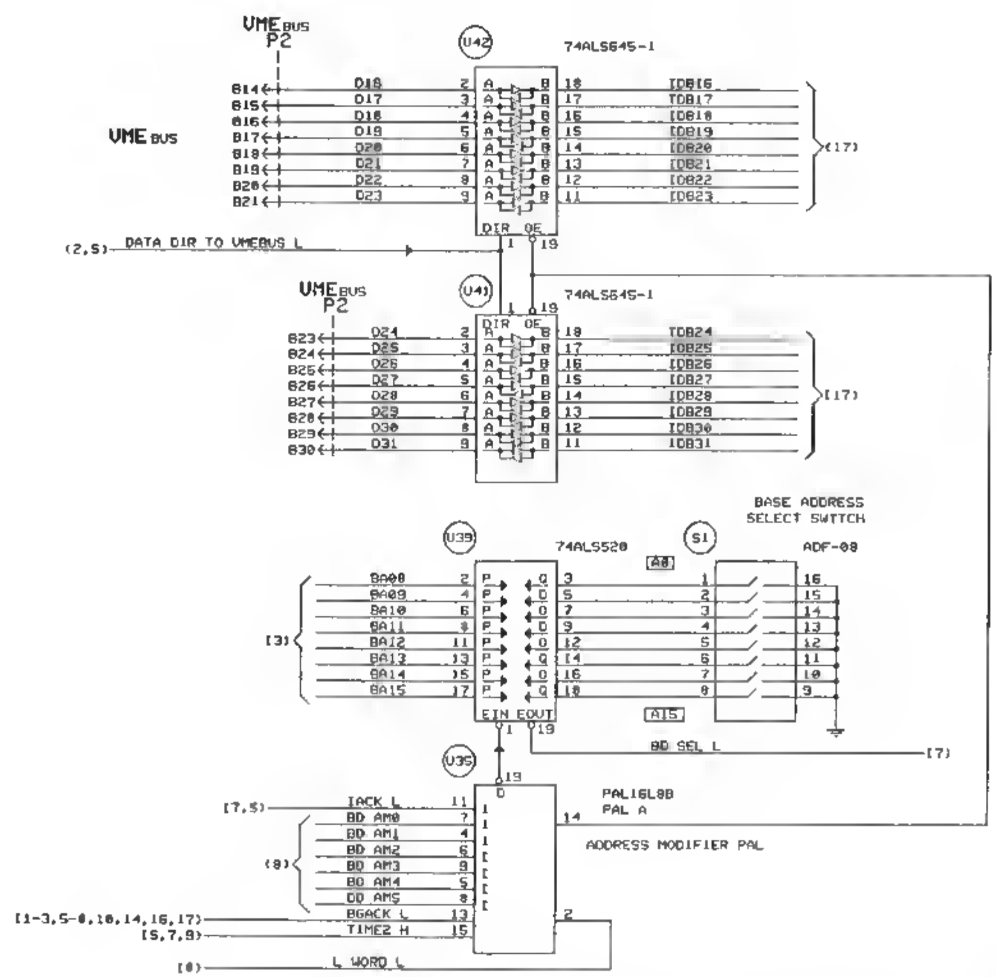


VMIC

SIGNATURES		DATE
DRAWN	C.A. Berry	9/29/89
CHECKED	A.E.D.	1-2-91

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308

SIZE		DWG NO.	REV.
B	0BPH5	141-000DMA-000	J
SCALE		SHEET	3



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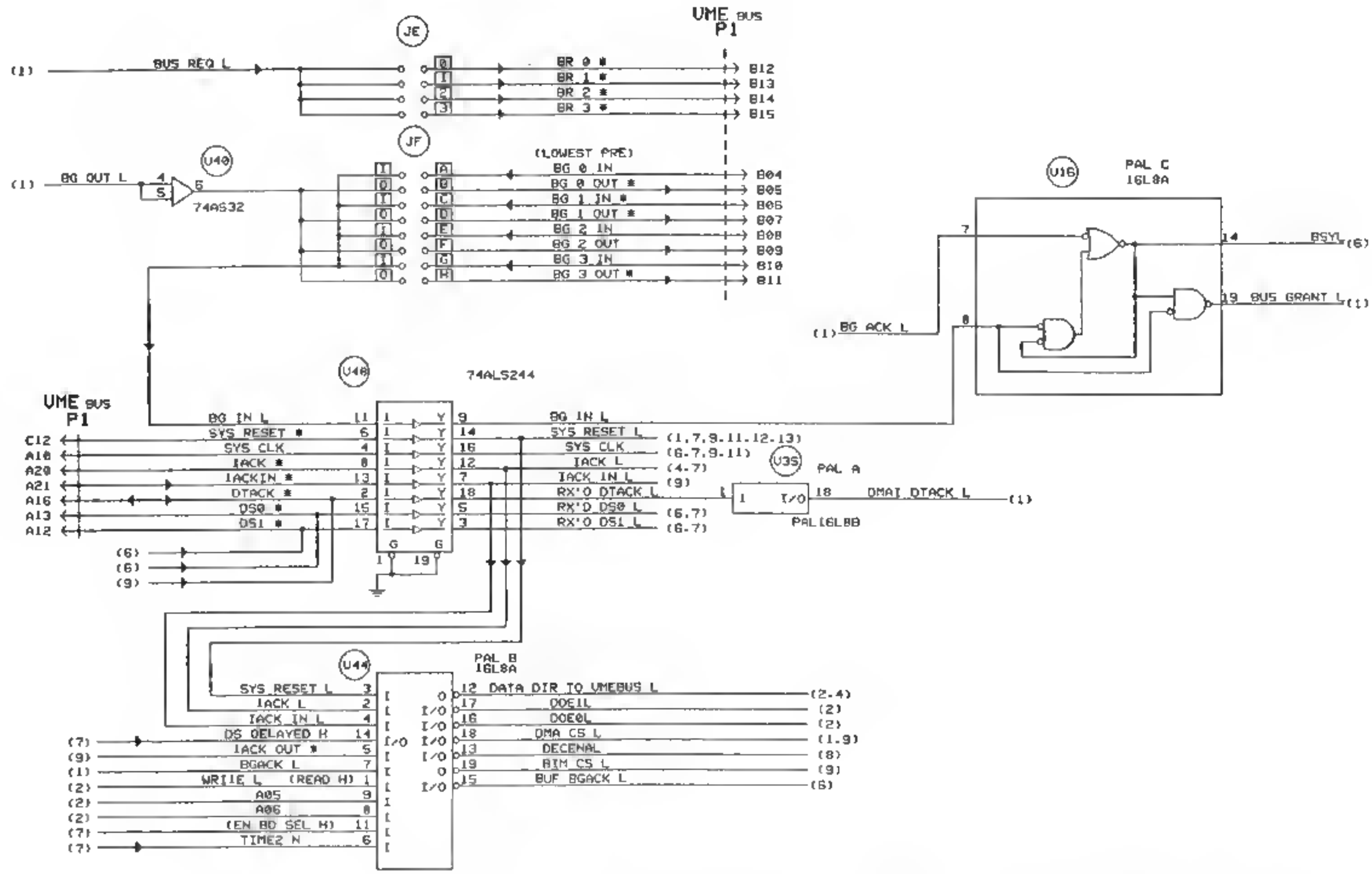
SIGNATURES		DATE
DRAWN	C.A. Berry	9/29/87
CHECKED	A.E.O.	1-2-91

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308

SIZE		DWG NO.	REV.
B	0BPH5	141-000DMA-000	J
SCALE			SHEET 4



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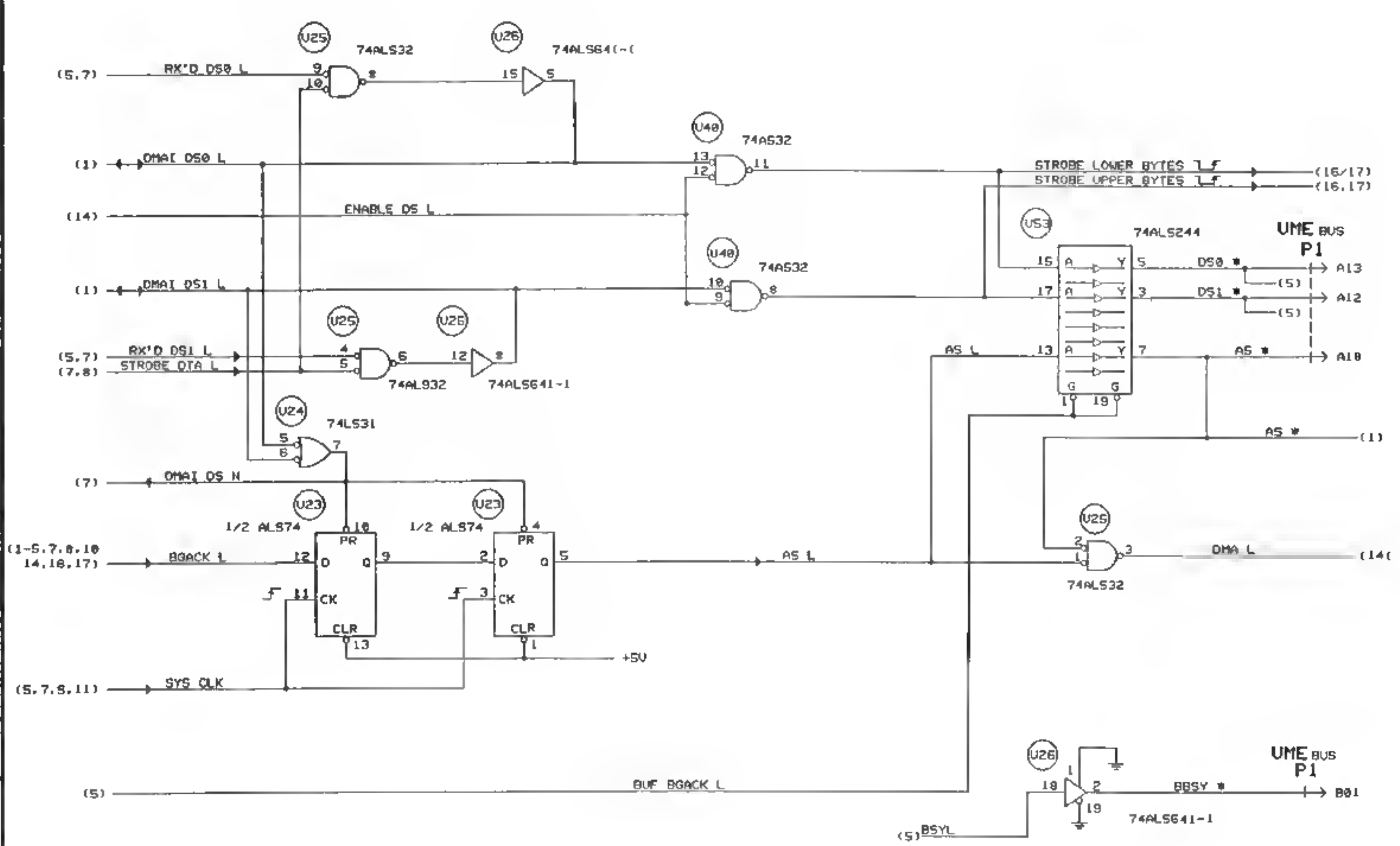
SIGNATURES		DATE
DRAWN	C.A. Berry	9/29/87
CHECKED	R.E.O.	1-2-91

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308

SIZE		DWG NO.	REV.
B	0BPH5	141-000DMA-000	K
SCALE		SHEET	5



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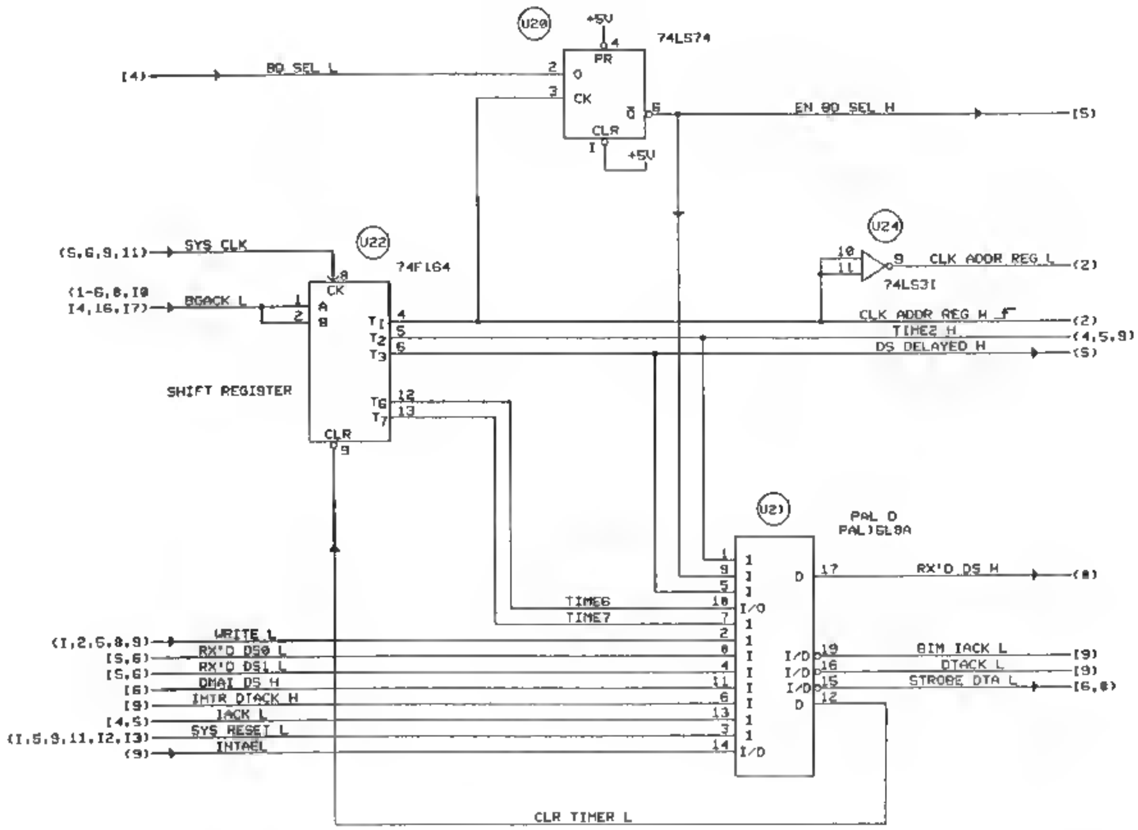
SIGNATURES		DATE
DRAWN	C.A. Berry	9/29/87
CHECKED		1-2-91

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308

SIZE		DWG NO.	REV.
B	0BPHS	141-000DMA-000	K
SCALE		SHEET	6



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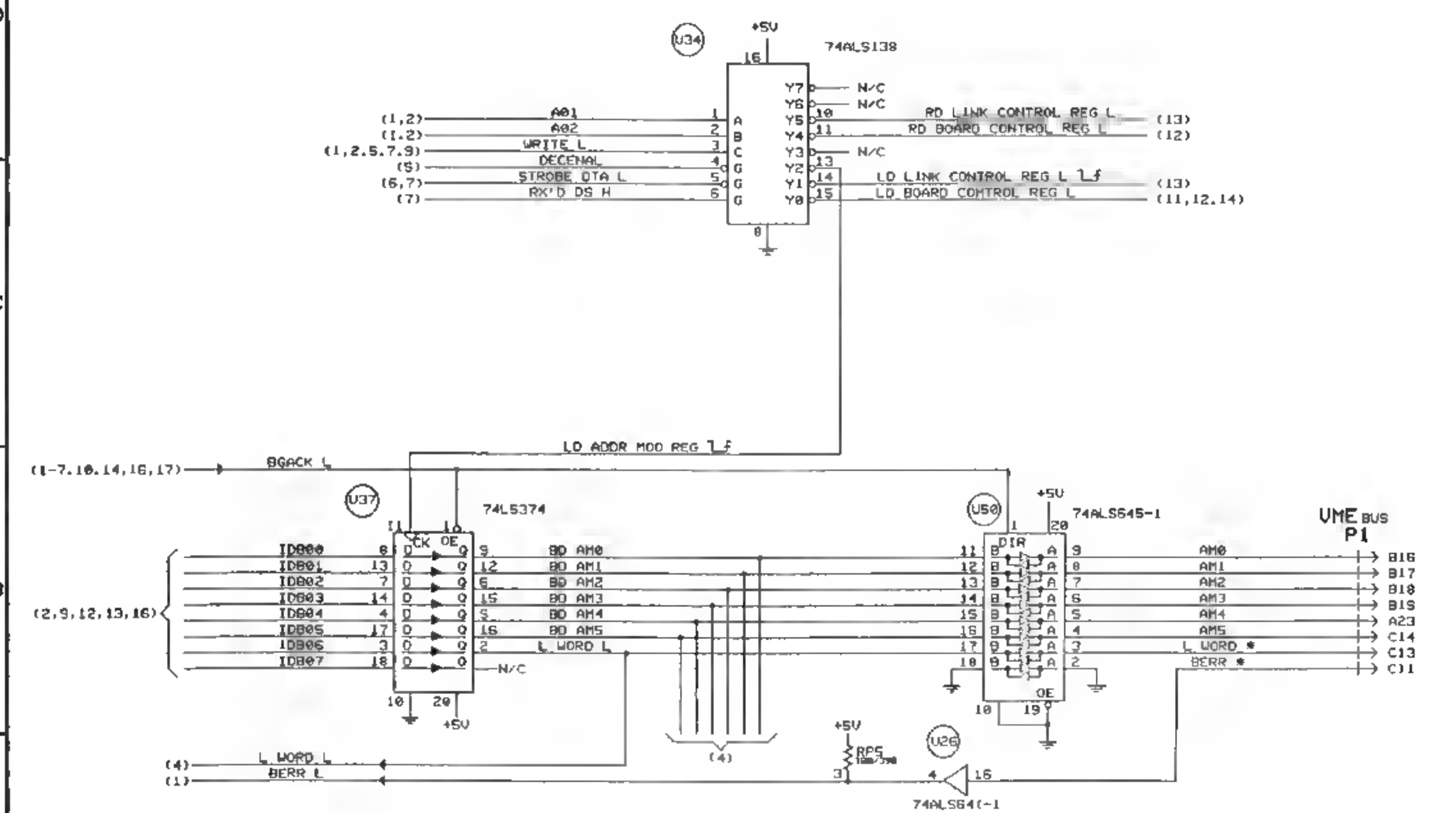
VMIC		VME MICROSYSTEMS INTERNATIONAL CORPORATION 12090 SOUTH MEMORIAL PARKWAY HUNTSVILLE, ALABAMA 35803-3308			
SIGNATURES	DATE	SIZE B	0BPH5	DWG NO. 141-000DMA-000	REV. J
DRAWN C.A. Berry	9/29/87	SCALE		SHEET 7	
CHECKED	1-2-91				



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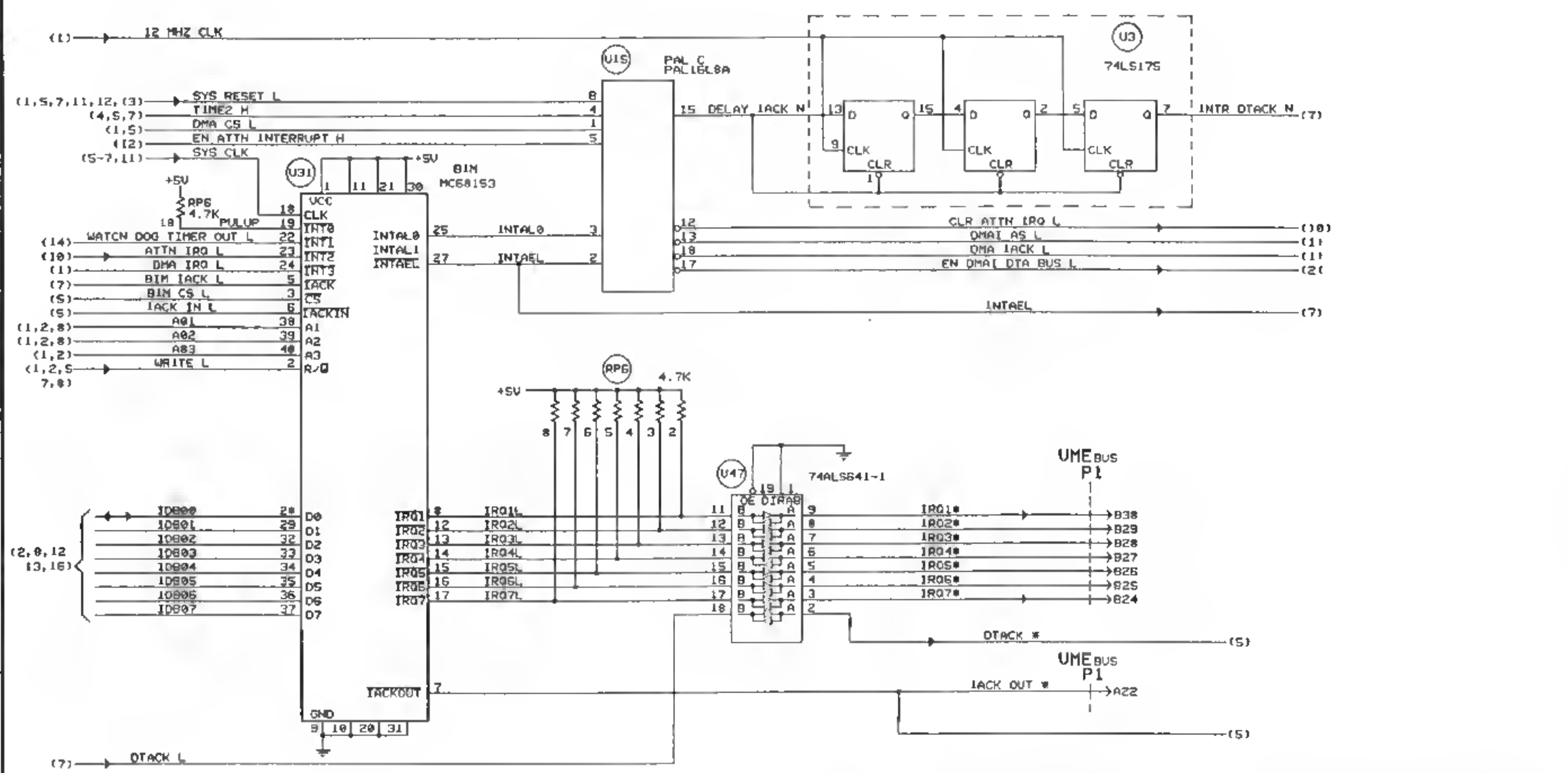
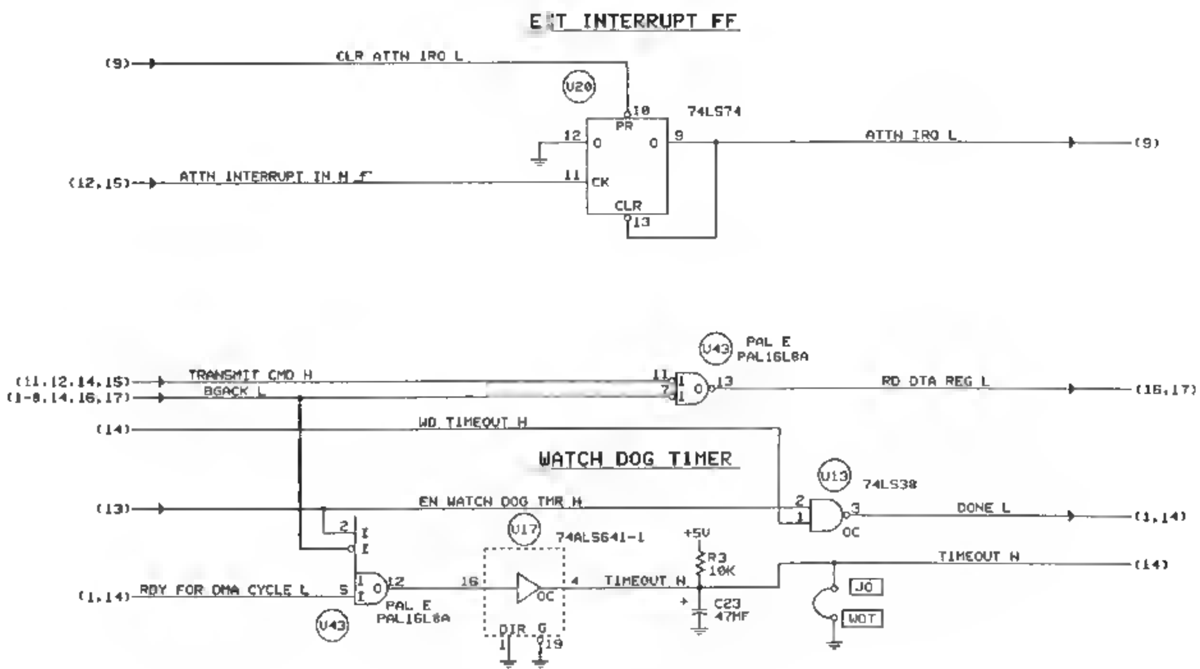
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308

SIGNATURES		DATE
DRAWN	C.A. Berry	9/29/87
CHECKED	[illegible]	1-2-[illegible]

SIZE		DWG NO.	REV.
B	0BPH5	141-000DMA-000	J
SCALE		SHEET	8



VMIC		VME MICROSYSTEMS INTERNATIONAL CORPORATION 12090 SOUTH MEMORIAL PARKWAY HUNTSVILLE, ALABAMA 35803-3308		
SIGNATURES	DATE	SIZE B	DWG NO. 141-000DMA-000	REV. J
DRAWN E.A. Berry	9/29/87	0BPH5		
CHECKED R.E.O.	1-2-91	SCALE		SHEET 9

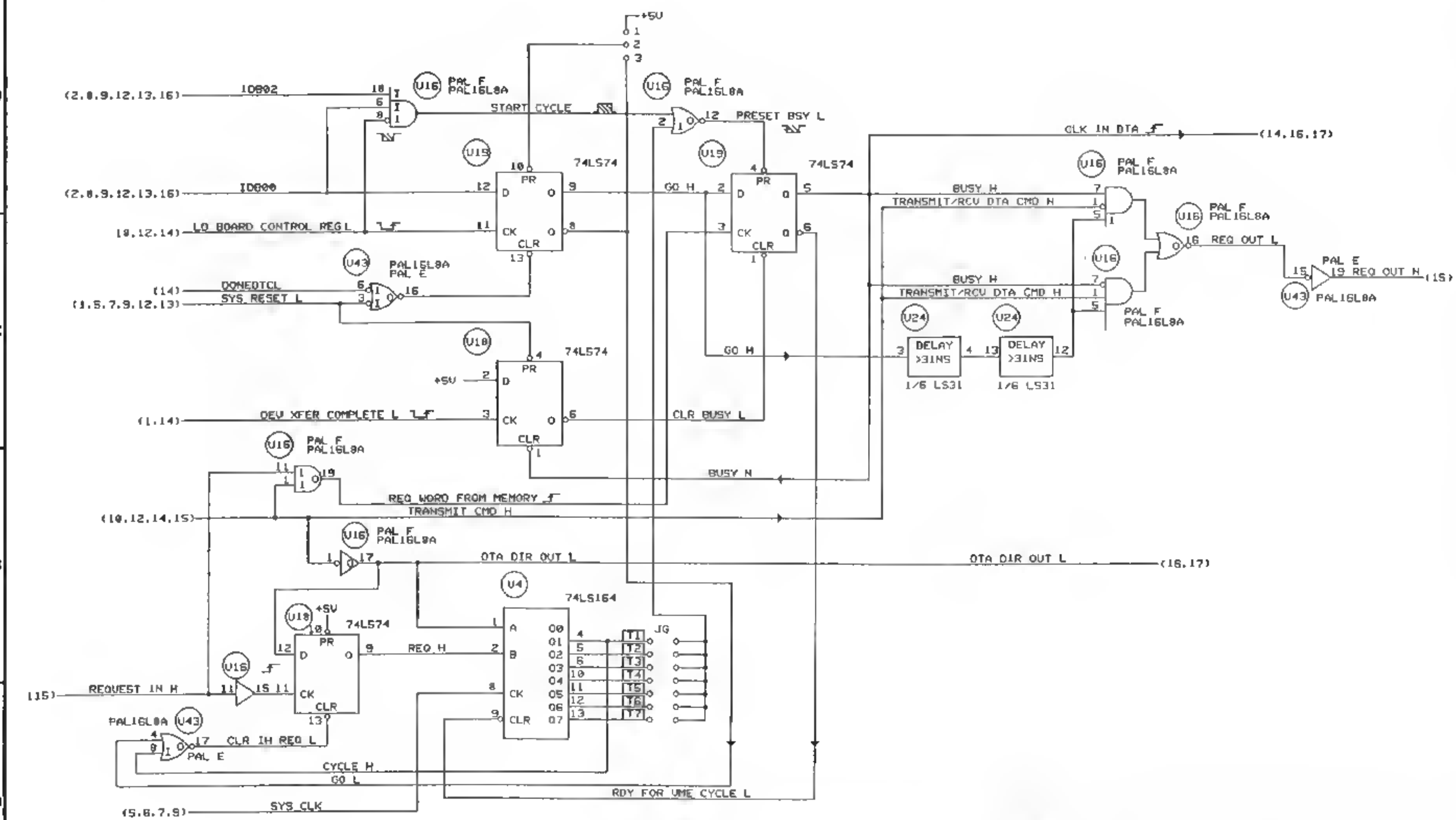


VMIC

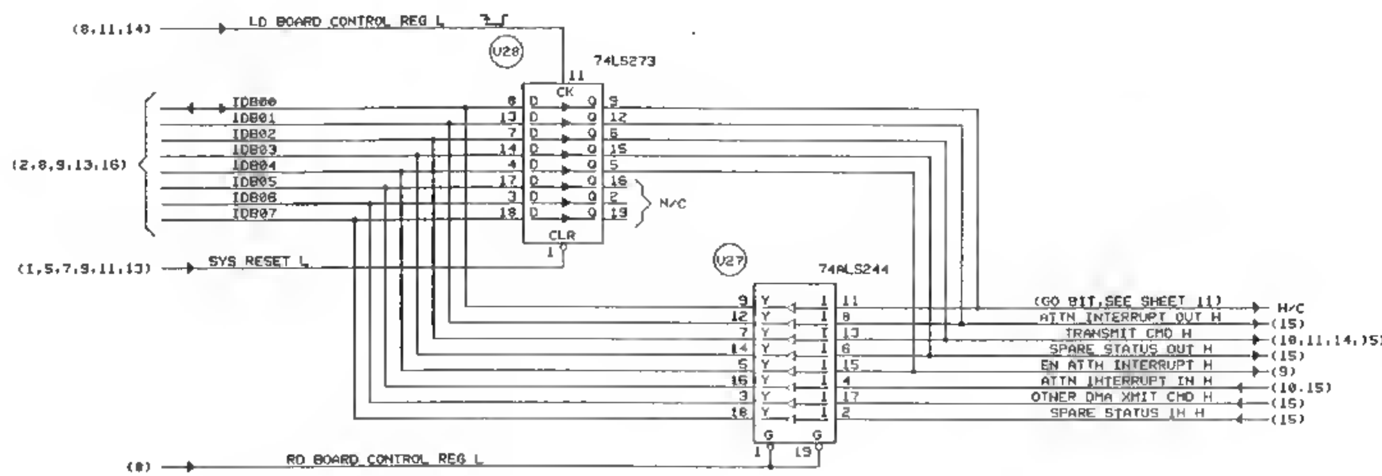
SIGNATURES		DATE
DRAWN	C.A. Berry	9/29/87
CHECKED	?.S.D.	1-2-91

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308

SIZE		DWG NO.	REV.
B	0BPHS	141-000DMA-000	J
SCALE			SHEET 18



VMIC		VME MICROSYSTEMS INTERNATIONAL CORPORATION 12090 SOUTH MEMORIAL PARKWAY HUNTSVILLE, ALABAMA 35803-3308			
SIGNATURES	DATE	SIZE		DWG NO.	REV.
DRAWN C A Berry	9/29/89	B	0BPH5	141-000DMA-000	K
CHECKED A.E.O.	1-4-90	SCALE			SHEET 11

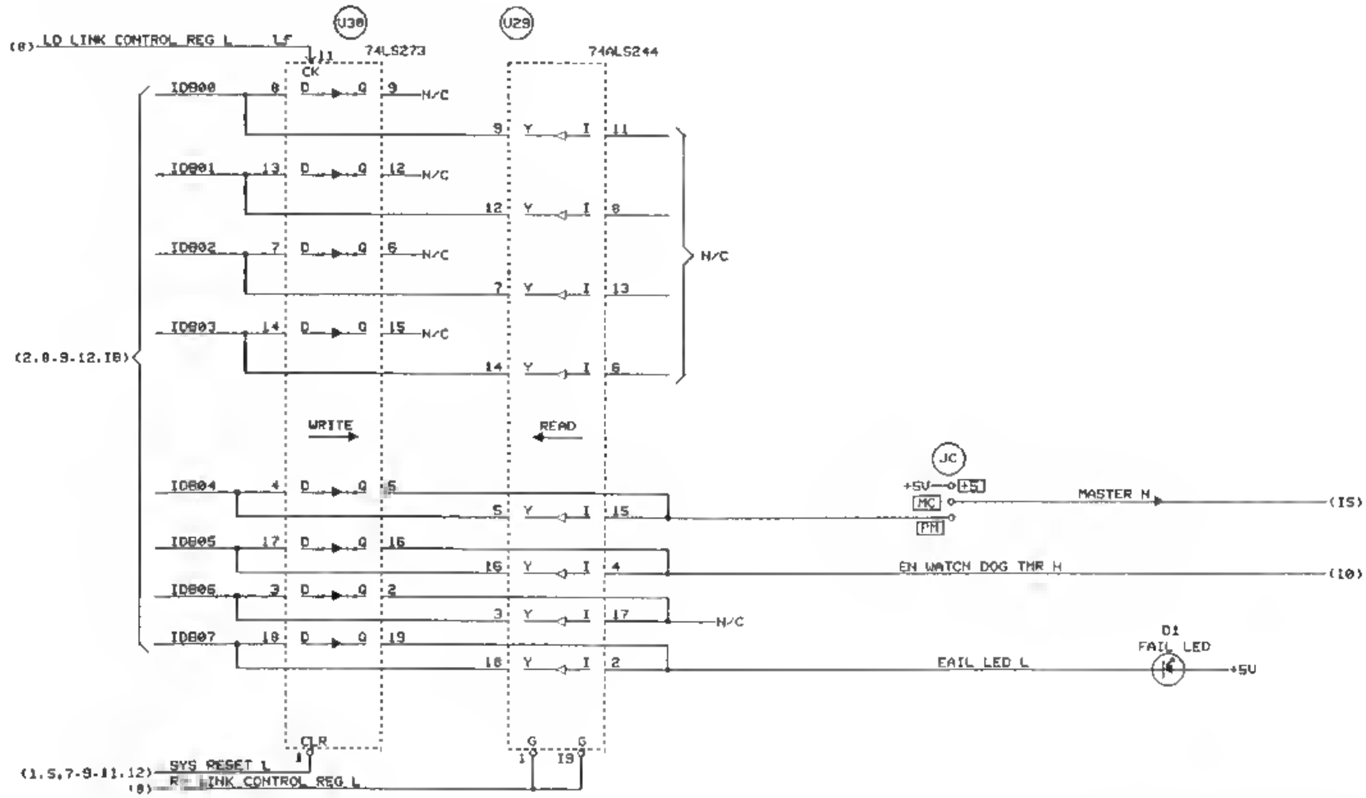


VMIC

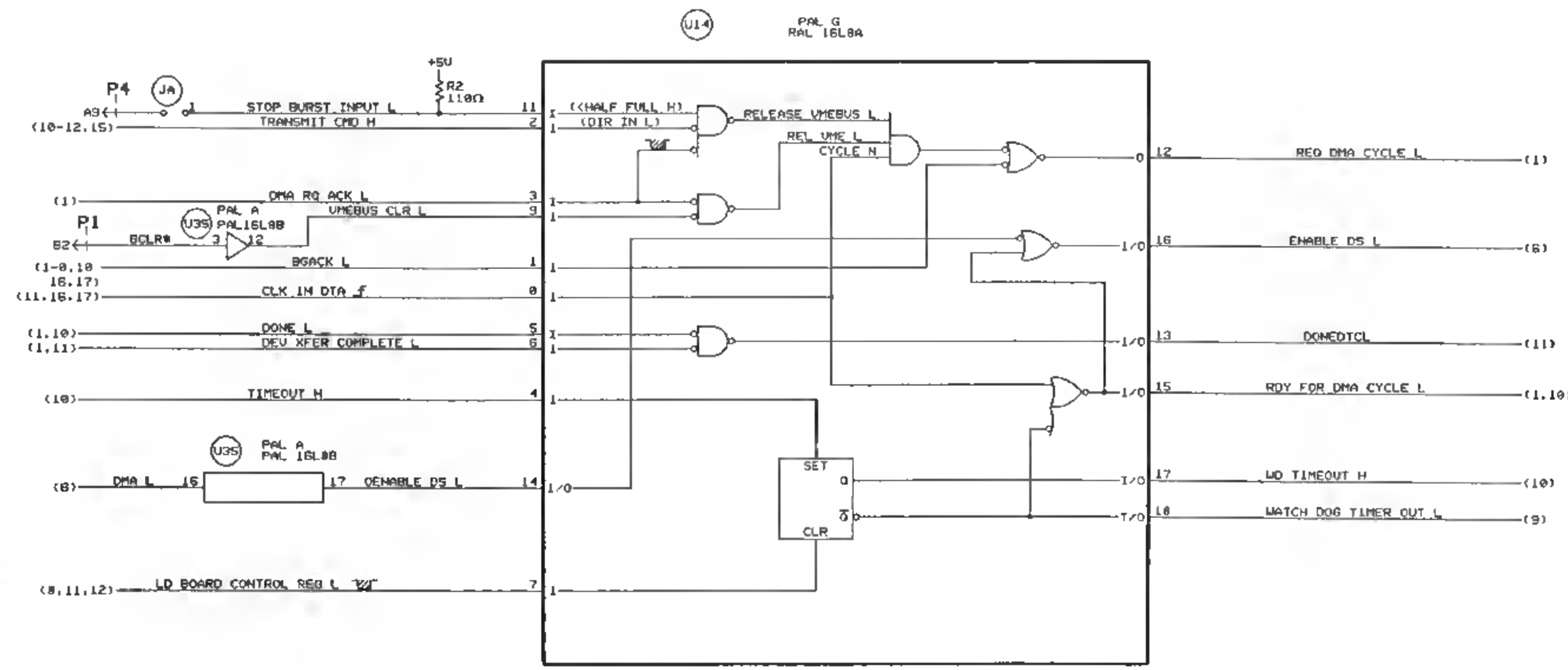
SIGNATURES		DATE
DRAWN	C A Berry	9/29/87
CHECKED	S. E. D.	1-2-91

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308

SIZE		DWG NO.	REV.
B	0BPHS	141-000DMA-000	J
SCALE			SHEET 12



VMIC		VME MICROSYSTEMS INTERNATIONAL CORPORATION 12090 SOUTH MEMORIAL PARKWAY HUNTSVILLE, ALABAMA 35803-3308		
SIGNATURES	DATE	SIZE B	DWG NO. 0BPH5 141-000DMA-000	REV. J
DRAWN C.A. Berry	9/29/87			
CHECKED A.E.O.	1-2-91	SCALE		SHEET 13



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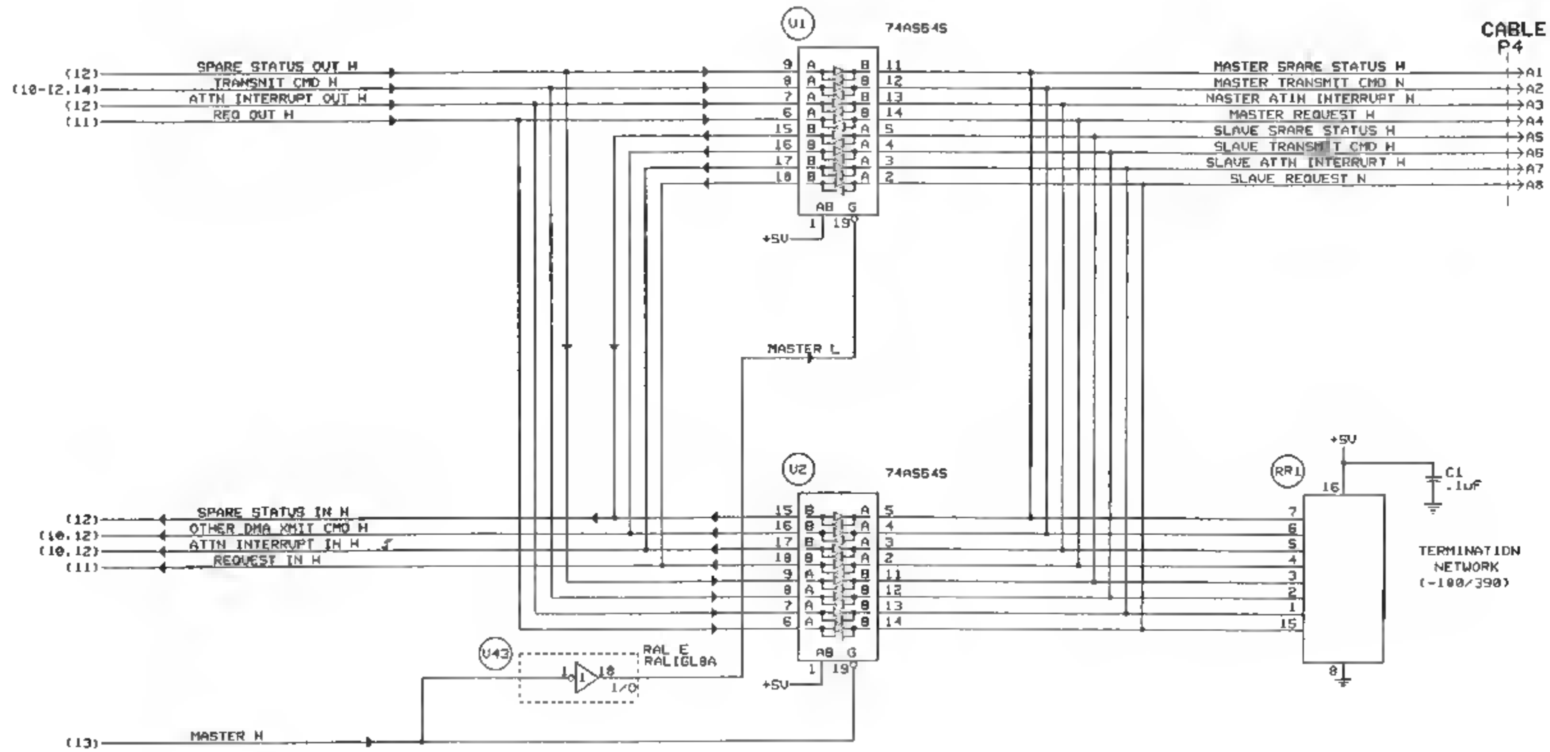
VMIC		VME MICROSYSTEMS INTERNATIONAL CORPORATION 12090 SOUTH MEMORIAL PARKWAY HUNTSVILLE, ALABAMA 35803-3308			
SIGNATURES	DATE	SIZE B	08PHS	DWG NO. 141-000DMA-000	REV. J
DRAWN C.A. Berry	9/29/87	SCALE		SHEET 14	
CHECKED R.E.O.	1-2-91				



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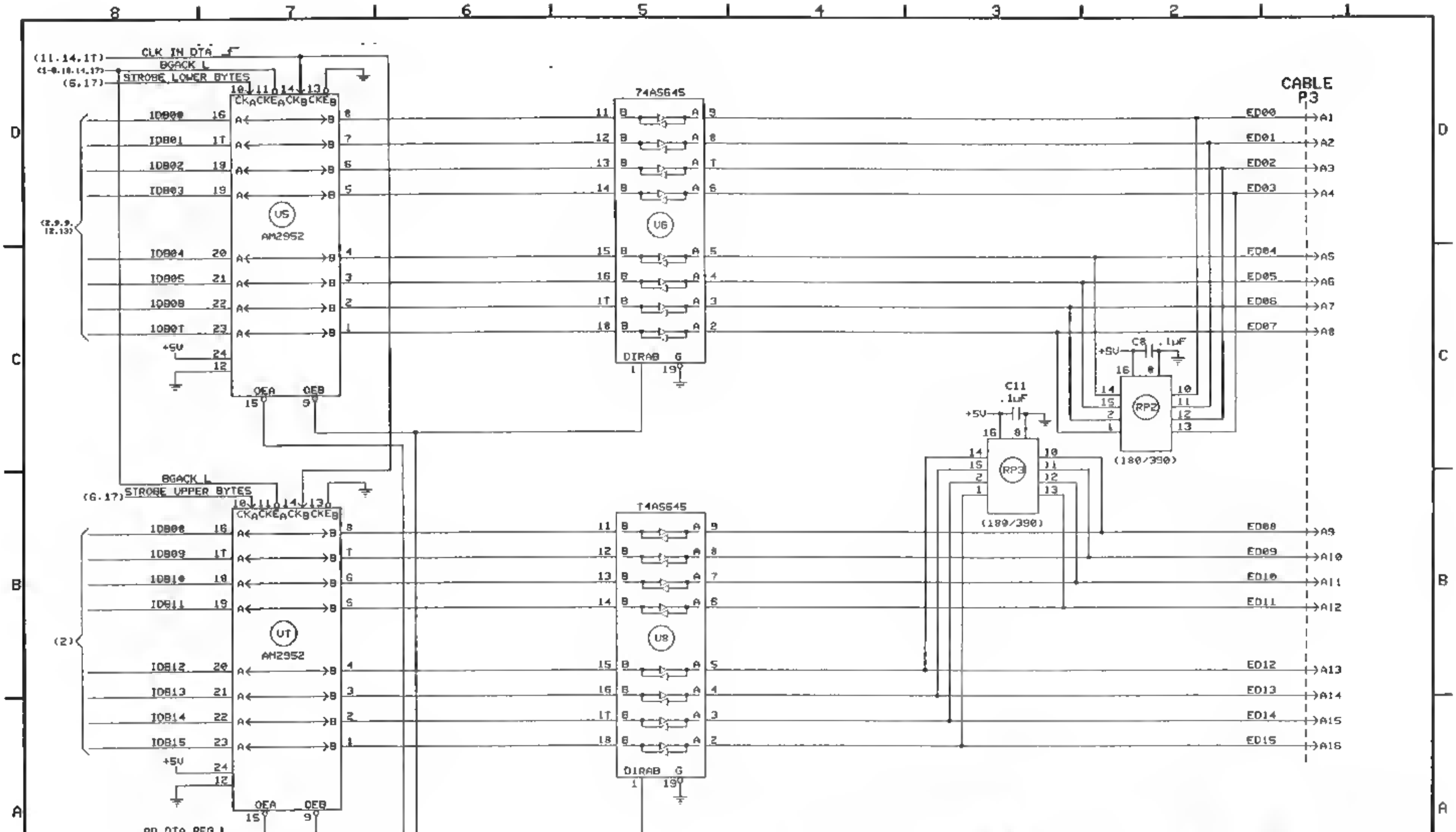
VMIC		VME MICROSYSTEMS INTERNATIONAL CORPORATION 12090 SOUTH MEMORIAL PARKWAY HUNTSVILLE, ALABAMA 35803-3308		
SIGNATURES	DATE			
DRAWN C.A. Berry	10/6/87	SIZE B 0BPHS	DWG NO. 141-000DMA-000	REV. K
CHECKED S.E.O.	1-2-91	SCALE		SHEET 15



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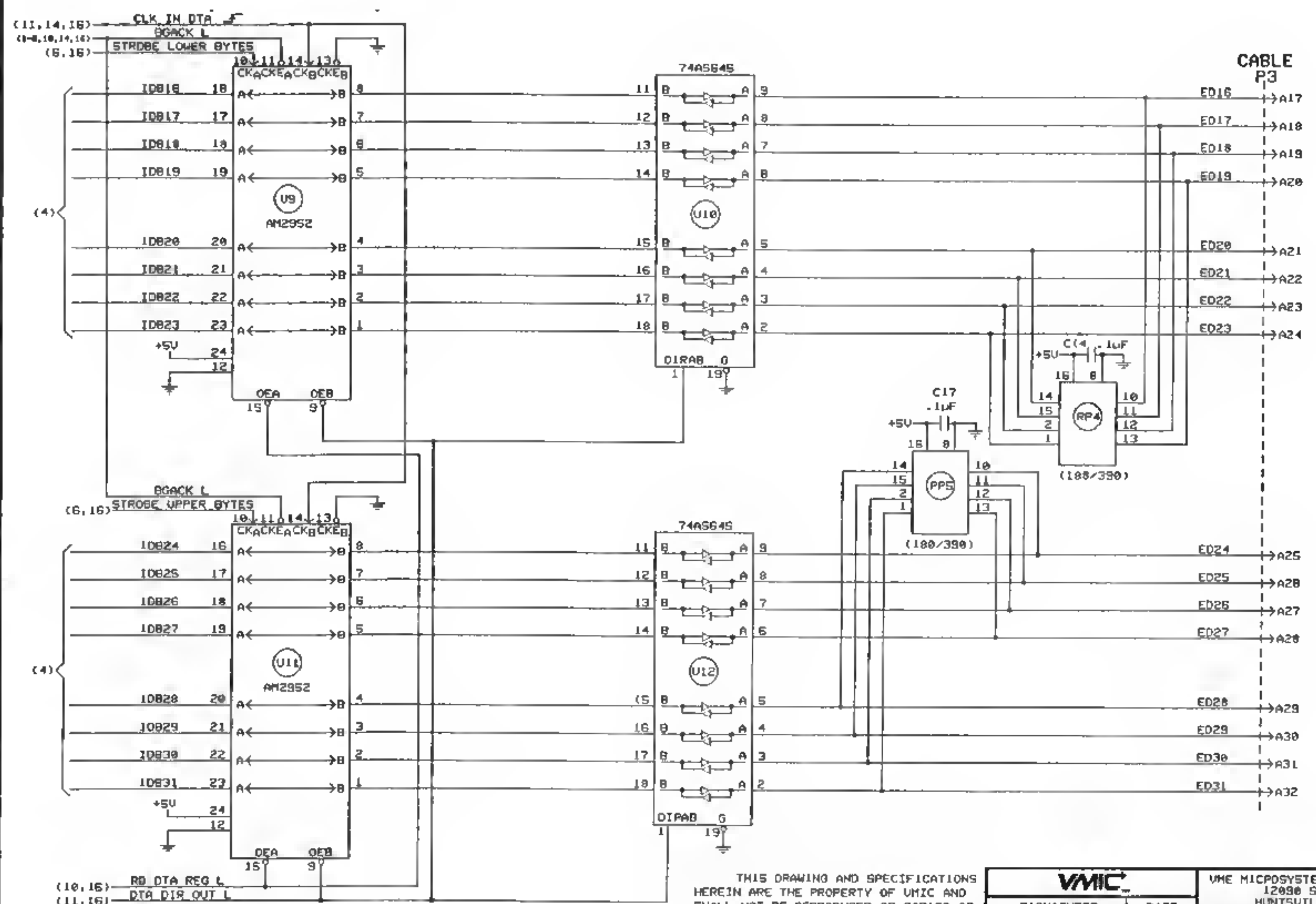
VMIC		VME MICROSYSTEMS INTERNATIONAL CORPORATION 12090 SOUTH MEMORIAL PARKWAY HUNTSVILLE, ALABAMA 35803-3308			
SIGNATURES	DATE	SIZE		DWG NO.	REV.
DRAWN C.A. Berry	10/09/87	B	0BPH5	141-000DMA-000	J
CHECKED	1-2-91	SCALE		SHEET	16



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DRAWN C.A. Derry	10/09/87	SCALE		SHEET 17 OF 17
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APPENDIX B

INTEGRATED CIRCUIT TECHNICAL SPECIFICATIONS

DESCRIPTION	PART NO.
Bus Interrupt Module	MC68153
Direct Memory Access Interface	SCB68430

MOTOROLA
SEMICONDUCTORS
PO BOX 20912 • PHOENIX ARIZONA 85036

MC68153

Advance Information

BUS INTERRUPTER MODULE

The bipolar LSI MC68153 Bus Interrupter interfaces a microcomputer system bus to multiple slave devices requiring interrupt capabilities. It handles up to 4 independent sources of interrupt requests and is fully programmable.

- VERSAbus/VMEbus Compatible
- MC68000 Compatible
- Handles 4 Independent Interrupt Sources
- 8 Programmable Read/Write Registers
- Programmable Interrupt Request Levels
- Programmable Interrupt Vectors
- Supports Interrupt Acknowledge Daisy Chain
- Control Registers Contain Flag Bits
- Single +5.0 Volt Supply
- Total Power Dissipation = 1.5 W Typical
- Temperature Range of 0°C to 70°C
- Chip Access Time = 200 ns Typical with 16 MHz Clock
- 40-Pin Dual-In-Line Package

TTL

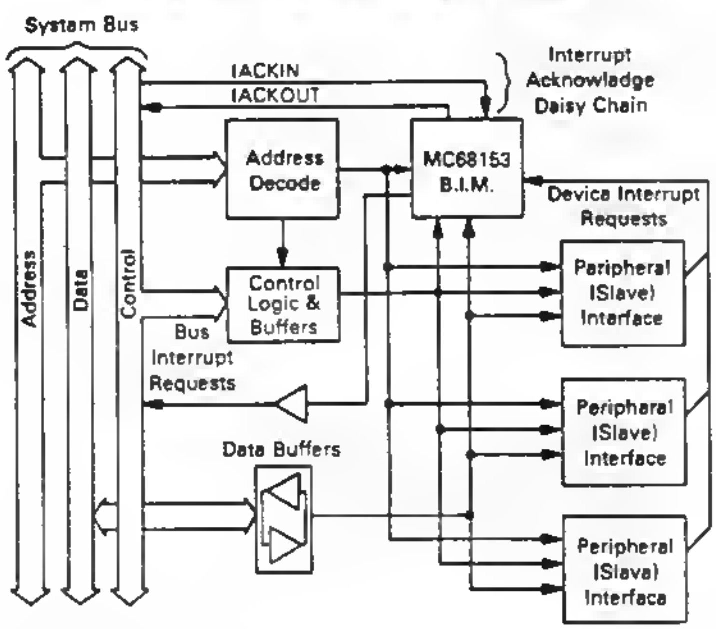
BUS INTERRUPTER MODULE

ADVANCED LOW POWER SCHOTTKY

P SUFFIX
PLASTIC PACKAGE
CASE 711-03

L SUFFIX
CERAMIC PACKAGE
CASE 734-04

FIGURE 1 — MC68153 SYSTEM BLOCK DIAGRAM



VERSAbus is a trademark of Motorola.

PIN ASSIGNMENTS

Signal	Pin	Pin	Signal
V_{CC}	1	40	A3
R/$\overline{W}$	2	39	A2
$\overline{CS}$	3	38	A1
$\overline{DTACK}$	4	37	D7
$\overline{IACK}$	5	36	D6
$\overline{IACKIN}$	6	35	D5
$\overline{IACKOUT}$	7	34	D4
$\overline{IRQ1}$	8	33	D3
GND	9	32	D2
GND	10	31	GND
V_{CC}	11	30	V_{CC}
$\overline{IRQ2}$	12	29	D1
$\overline{IRQ3}$	13	28	D0
$\overline{IRQ4}$	14	27	$\overline{INTAE}$
$\overline{IRQ5}$	15	26	INTAL1
$\overline{IRQ6}$	16	25	INTAL0
$\overline{IRQ7}$	17	24	$\overline{INT3}$
CLK	18	23	$\overline{INT2}$
$\overline{INT0}$	19	22	$\overline{INT1}$
GND	20	21	V_{CC}

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ADI-1057

ABSOLUTE MAXIMUM RATINGS (Beyond which useful life may be impaired.)

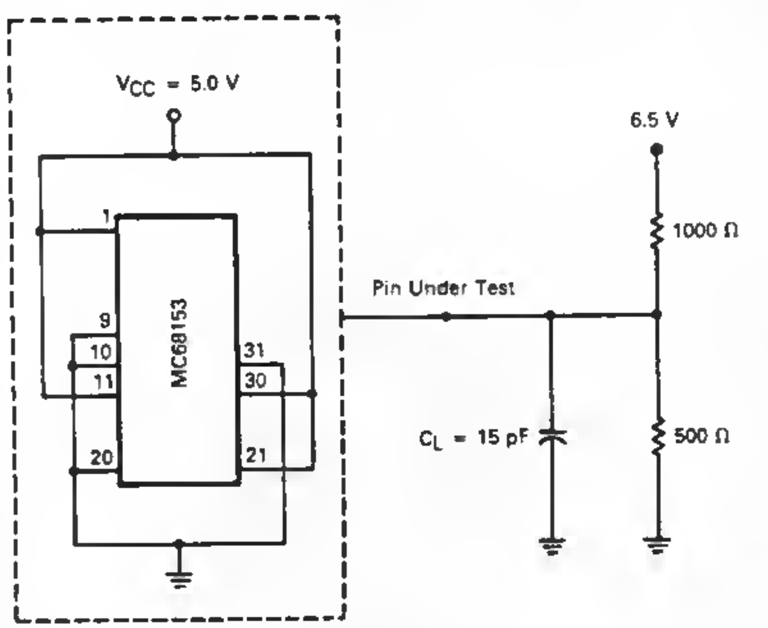
Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{in}	−0.5 to +7.0	V
Input Current	I_{in}	−30 to +5.0	mA
Output Voltage	V_{out}	−0.5 to +5.5	V
Output Current	I_{OL}	Twice Rated I_{OL}	mA
Storage Temperature	T_{stg}	−65 to +140	°C
Junction Operating Temperature	T_J	−55 to +140	°C

BURN-IN LIMITS: A maximum T_J of +175°C may be used for periods not to exceed 250 hours.

DC ELECTRICAL SPECIFICATIONS (V_{CC} = 5.0 V ±5%, T_A = 0°C to 70°C)

Parameter	Symbol	Min	Max	Unit	Test Conditions
High Level Input Voltage	V_{IH}	2.0	—	V	
Low Level Input Voltage	V_{IL}	—	0.8	V	
Input Clamp Voltage	V_{IK}	—	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
High Level Output Voltage(1)	V_{OH}	2.7	—	V	V_{CC} = MIN, I_{OH} = −400 μA
Low Level Output Voltage	V_{OL}	—	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA
Output Short Circuit Current(2)	I_{OS}	−15	−130	mA	V_{CC} = MAX, V_{OUT} = 0 V
High Level Input Current	I_{IH}	—	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
Low Level Input Current	I_{IL}	—	−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
Supply Current	I_{CC}	225	385	mA	V_{CC} = MAX
Output Off Current (High)	I_{OZH}	—	20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V
Output Off Current (Low)	I_{OZL}	—	−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V

AC TEST CIRCUIT — AC Testing of All Outputs



NOTES:
1. Not applicable to open-collector outputs.
2. Not more than one output should be shorted at a time for longer than one second.
3. $\overline{CS}$ Low to CLK High (Setup Time) of 15 ns Min must be observed.
4. $\overline{IACK}$ Low to CLK High and $\overline{IACKIN}$ Low to CLK High (Setup Times) of 15 ns Min must be observed.
5. See Table 1 for additional performance guidelines.

AC ELECTRICAL SPECIFICATIONS (V_{CC} = 5.0 V ±5%, T_A = 0°C to 70°C)

Parameter	Test Number[5]	Max (ns)
CLK High to Data Out Valid (Delay)[3]	1	55
CLK High to $\overline{\text{DTACK}}$ Low (Delay)[3]	2	40
$\overline{\text{CS}}$ High to $\overline{\text{DTACK}}$ High (Delay)	3	35
CLK High to Data Out Valid (Delay)[4]	4	55
CLK High to $\overline{\text{INTAE}}$ Low (Delay)[4]	5	40
$\overline{\text{IACK}}$ High to Data Out High Impedance (Delay)	6	60
$\overline{\text{IACK}}$ High to $\overline{\text{DTACK}}$ High (Delay)	7	45
$\overline{\text{CS}}$ High to Data Out High (Delay)	8	45
CS High to IRQ High (Delay)	9	60
$\overline{\text{IACK}}$ High to $\overline{\text{INTAE}}$ High (Delay)	10	35

GENERAL DESCRIPTION

The MC68153 Bus Interrupter Module (BIM) is designed to serve as an interrupt requester for peripheral devices in a microcomputer system. Up to 4 independent devices can be interfaced to the system bus by the MC68153. Intended for asynchronous master/slave bus operation, the BIM is compatible with VERSAbus, VMEbus, MC68000 device bus, and other system buses. Figure 1 shows a block diagram of a typical configuration. In this example, three peripheral devices (bus slaves) are connected to the system data bus. Each of these devices could be parallel I/O, serial I/O, or some other function. An interrupt request from any device is routed to the MC68153, and the BIM handles all interface to the system bus. It generates a bus interrupt request as a result of the device interrupt request. When the system interrupt handler or processor responds with an interrupt acknowledge cycle, the MC68153 can answer supplying an interrupt vector and handling all timing.

The functional block diagram of the MC68153 is shown in Figure 2. The device contains circuitry to accept four separate interrupt sources ($\overline{\text{INT0}}$ – $\overline{\text{INT3}}$). Interface to the system bus includes generation of bus interrupt requests ($\overline{\text{IRQ1}}$ – $\overline{\text{IRQ7}}$), response to a bus interrupt acknowledge cycle (either supplying a vector or passing on a daisy chain signal), and releasing the bus interrupt request signal at the proper time. The BIM has flexibility provided by eight programmable read/write registers. Four 8-bit vector registers (VR0 – VR3) contain status/address information and supply a byte vector in response to an interrupt acknowledge cycle for the corresponding interrupt source. Four other 8-bit control registers (CR0 – CR3) contain information that oversees operation of the interrupt circuitry. The control information is programmable and includes interrupt request level and interrupt enable and disable. Also contained in the control registers are flag-bits. These flags are useful for task coordination, resource management, and interprocessor communication.

SIGNAL DESCRIPTION

Throughout the data sheet, signals are presented using the terms asserted and negated independent of whether the signal is asserted in the high voltage or low voltage state. Active low signals are denoted by a superscript bar.

BIDIRECTIONAL DATA BUS — D0 – D7

Pins D0 – D7 form an 8-bit bidirectional data bus to/from the system bus. These are active high, 3-state pins. D7 is the most significant bit.

ADDRESS INPUTS — A1 – A3

These active high inputs serve two functions. One function is to select one of the eight possible registers during a read or write cycle. Secondly, during an interrupt acknowledge A1 – A3 show the level of interrupt being acknowledged, and the BIM uses these to determine if a match exists with an internal level.

CHIP SELECT — $\overline{\text{CS}}$

$\overline{\text{CS}}$ is an active low input used to select the BIM's registers for the current bus cycle. Address strobe, data strobe, and appropriate address bits must be included in the chip select equation.

READ/WRITE — R/$\overline{\text{W}}$

The R/$\overline{\text{W}}$ input is a signal from the system bus used to determine if the current bus cycle is a read (high) or write (low).

DATA TRANSFER ACKNOWLEDGE — $\overline{\text{DTACK}}$

$\overline{\text{DTACK}}$ is an open-collector, active low output that signals the completion of a read, write, or interrupt acknowledge cycle. During read or interrupt acknowledge cycles, $\overline{\text{DTACK}}$ is asserted by the MC68153 after data has been provided on the data bus; during write cycles it is asserted after data has been accepted from the data bus. A pullup resistor is required to maintain $\overline{\text{DTACK}}$ high between bus cycles.

FIGURE 2 — MC68153 FUNCTIONAL BLOCK DIAGRAM

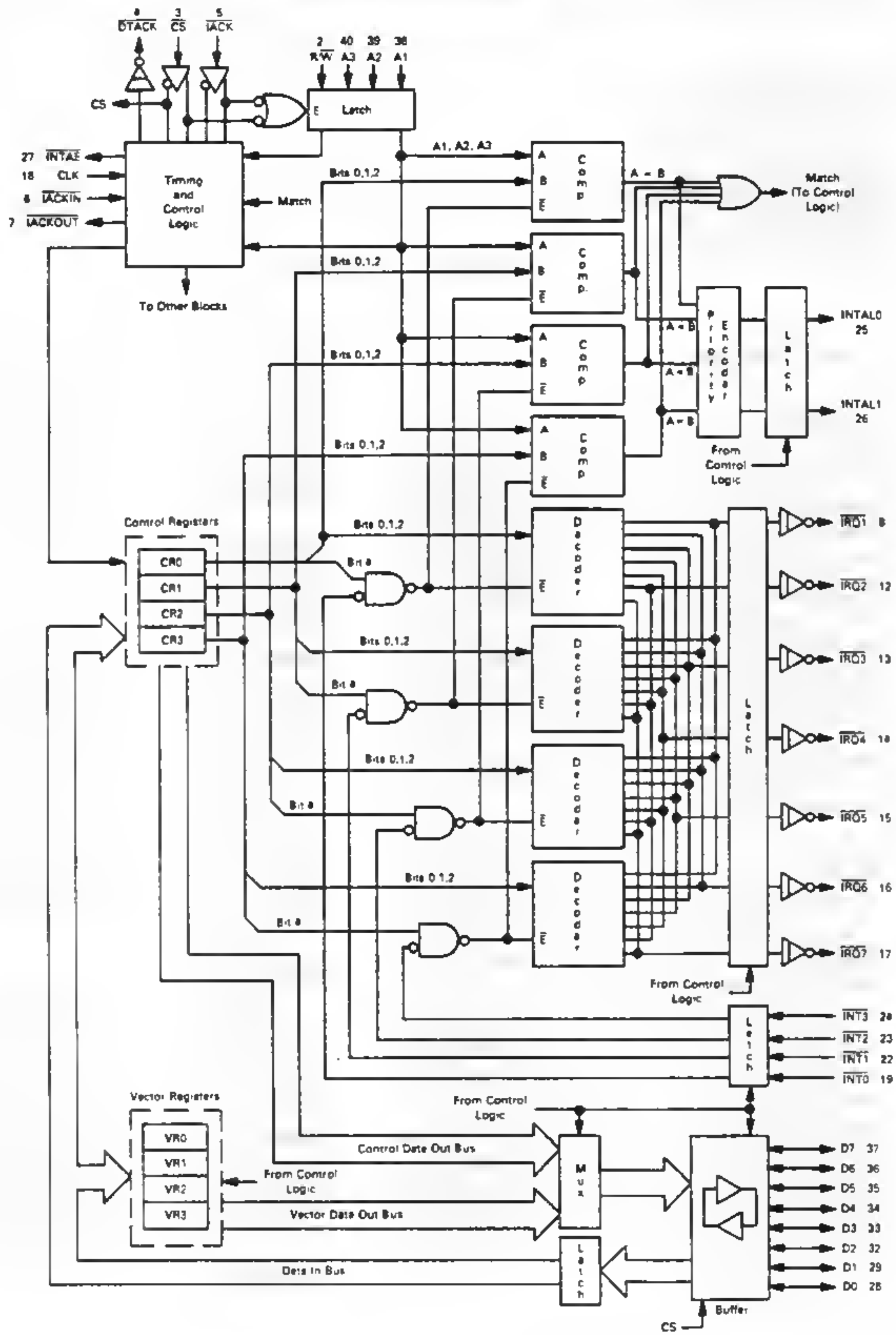
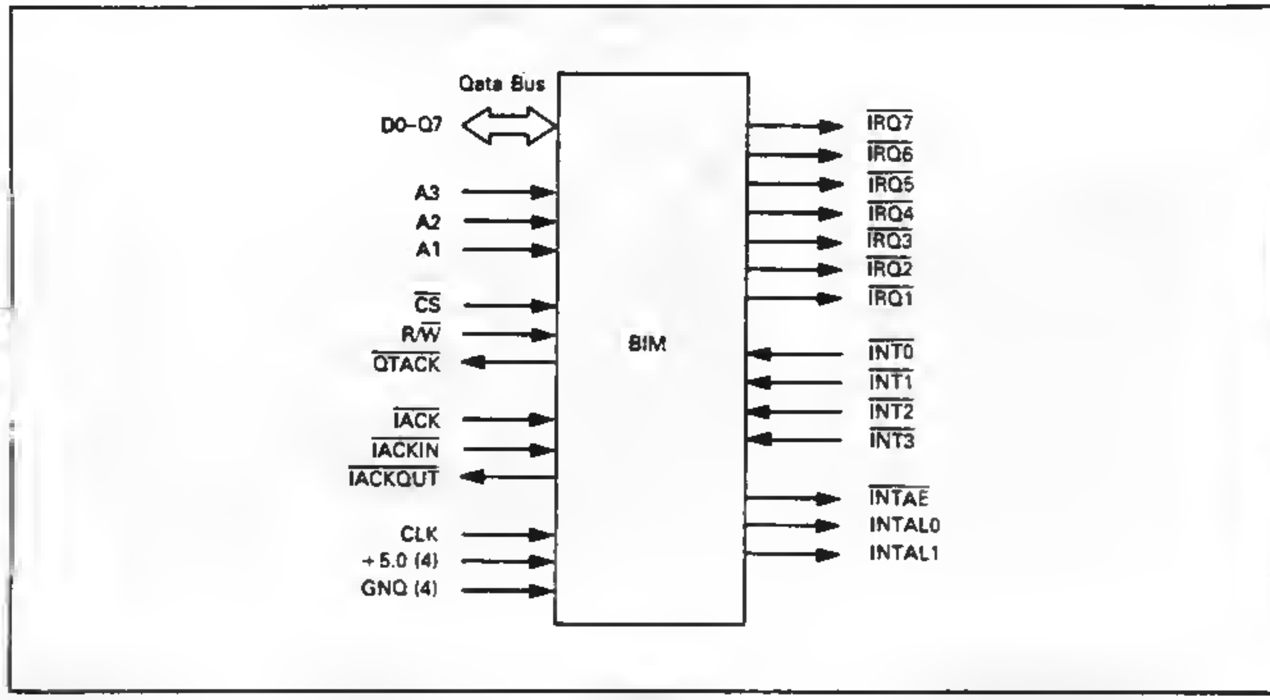


FIGURE 3 — LOGICAL PIN ASSIGNMENT



INTERRUPT ACKNOWLEDGE SIGNALS — IACK, IACKIN, IACKOUT

These three pins support the interrupt acknowledge cycle. A low level on the IACK input indicates an interrupt acknowledge cycle has been initiated. This signal is conditioned externally with Address Strobe and the lower data strobe of an MC68000 type bus. After IACK is asserted the BIM compares the interrupt level presented on address lines A1, A2, and A3 with the current levels generated internally and determines if a match exists. Then, if input IACKIN is asserted (driven low), the BIM will either complete the interrupt acknowledge cycle if a match exists or assert output IACKOUT if no match exists.

IACKIN and IACKOUT form part of a prioritized interrupt acknowledge daisy chain. The daisy chain prioritizes interrupters and guarantees that two or more devices requesting an interrupt on the same level will not respond to the same cycle. The requesting device (or interrupter) must wait until IACKIN is asserted and not pass the signal on (assert IACKOUT) if it is to complete the interrupt acknowledge cycle.

BUS INTERRUPT REQUEST SIGNALS — IRQ1 - IRQ7

These open-collector outputs are low when asserted, indicating a bus interrupt is requested at the corresponding level. An open-collector buffer is normally required for sufficient drive when interfacing to a system bus. A pullup resistor is required to maintain IRQ1 - IRQ7 high between interrupt requests.

DEVICE INTERRUPT REQUEST SIGNALS — INT0 - INT3

INT0 - INT3 are active low inputs used to indicate to the BIM that a device wants a bus interrupt.

INTERRUPT ACKNOWLEDGE ENABLE — INTAE

During an interrupt acknowledge cycle, this output pin is asserted low to indicate that outputs INTAL0 and INTAL1 are valid. These two outputs contain an encoded number (x) corresponding to the interrupt (INTx) being acknowledged. This feature can be used to signal interrupting devices, which supply their own vector, when to respond to the interrupt acknowledge cycle with the vector and a DTACK signal.

INTERRUPT ACKNOWLEDGE LEVEL — INTAL0, INTAL1

These active high outputs contain an encoded number corresponding to the interrupt level being acknowledged. They are valid only when INTAE is asserted low.

CLOCK — CLK

The CLK input is used to supply the clock for internal operations of the MC68153.

RESET — CS, IACK

Although a reset input is not supplied, an on-board reset is performed if CS and IACK are asserted simultaneously.

FIGURE 4 — MC68153 REGISTER MODEL

ADDRESS BIT			FLAG	FLAG AUTO-CLEAR	EXTERNAL/$\overline{\text{INTERNAL}}$	INTERRUPT ENABLE	INTERRUPT AUTO-CLEAR	INTERRUPT LEVEL			
A3	A2	A1									
0	0	0	F	FAC	X/$\overline{\text{IN}}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 0
0	0	1	F	FAC	X/$\overline{\text{IN}}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 1
0	1	0	F	FAC	X/$\overline{\text{IN}}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 2
1	1	1	F	FAC	X/$\overline{\text{IN}}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 3
1	0	0	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 0
1	0	1	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 1
1	1	0	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 2
1	1	1	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 3
			7	6	5	4	3	2	1	0	REGISTER NAME
			REGISTER BIT								

REGISTER DESCRIPTION

The MC68153 contains 8 programmable read/write registers. There are four control registers (CR0 – CR3) that govern operation of the device. The other four (VR0 – VR3) are vector registers that contain the vector data used during an interrupt acknowledge cycle. Figure 4 illustrates the device register model.

CONTROL REGISTERS

There is a control register for each interrupt source, i.e., CR0 controls $\overline{\text{INT0}}$, CR1 controls $\overline{\text{INT1}}$, etc. The control registers are divided into several fields:

1. Interrupt level (L2, L1, L0) — The least significant 3-bit field of the register determines the level at which an interrupt will be generated:

L2	L1	L0	IRQ LEVEL
0	0	0	DISABLED
0	0	1	IRQ1
0	1	0	IRQ2
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

   A value of zero in the field disables the interrupt.

2. Interrupt Enable (IRE) — This field (Bit 4) must be set (high level) to enable the bus interrupt request associated with the control register. Thus, if the $\overline{\text{INTX}}$ line is asserted and IRE is cleared, *no* interrupt request ($\overline{\text{IRQX}}$) will be asserted.
3. Interrupt Auto-Clear (IRAC) — If the IRAC is set (Bit 3), IRE (Bit 4) is cleared during an interrupt acknowledge cycle responding to this request. This action of clearing IRE disables the interrupt request. To re-enable the interrupt associated with this register, IRE must be set again by writing to the control register.
4. External/Internal (X/$\overline{\text{IN}}$) — Bit 5 of the control register determines the response of the MC68153 during an interrupt acknowledge cycle. If the X/$\overline{\text{IN}}$ bit is clear (low level) the BIM will respond with vector data and a $\overline{\text{DTACK}}$ signal, i.e., an internal response. If X/$\overline{\text{IN}}$ is set, the vector is not supplied and no $\overline{\text{DTACK}}$ is given by the BIM, i.e., an external device should respond.
5. Flag (F) — Bit 7 is a flag that can be used in conjunction with the test and set instruction of the MC68000. It can be changed without affecting chip operation. It is useful for processor-to-processor communication and resource allocation.
6. Flag Auto-Clear (FAC) — If FAC (Bit 6) is set, the Flag bit is automatically cleared during an interrupt acknowledge cycle.

VECTOR REGISTERS

Each interrupt input has its own associated vector register. Each register is 8 bits wide and supplies a data byte during its interrupt acknowledge cycle if the associated External/Internal (X/$\overline{\text{IN}}$) control register bit is clear (zero). This data can be status, identification, or address information depending on system usage. The information is programmed by the system user.

DEVICE RESET

When the MC68153 is reset, the registers are set to a known condition. The control registers are set to all zeros (low). The vector registers are set to $0F. This value is the MC68000 vector for an uninitialized interrupt vector.

FUNCTIONAL DESCRIPTION

SYSTEM OVERVIEW

The MC68153 can be used with many system buses, however, it is primarily intended for VMEbus, VERSAbus and MC68000 applications. Figure 5 shows a system configuration similar to VMEbus. In the figure only one system Data Transfer Bus (DTB) master is used. The Priority Interrupt structure provides a means for peripheral slave devices to ask for an interrupt of other processor (DTB master) activity and receive service from the processor. The MC68153 BIM acts as an interface device requesting and responding to interrupt acknowledge cycles for up to 4 independent slaves.

In Figure 5, functional modules are identified as Interrupters and an Interrupt Handler. An Interrupter (such as the MC68153) receives slave requests for an interrupt and handles all interface to the system bus required to ask for and respond to interrupt requests. The Interrupt Handler receives the bus interrupt requests, determines when an interrupt acknowledge will occur and at which level, and finally either performs the interrupt acknowledge (IACK) cycle or tells the DTB master to execute the IACK cycle.

The signal lines in the Priority Interrupt structure include (* — indicates active low):

1. IRQ1*–IRQ7* — seven prioritized interrupt request lines.
2. IACK* — signal line that indicates an interrupt acknowledge cycle is occurring.
3. IACKIN*/IACKOUT* — two signals that form part of a daisy chain that prioritize interrupters.

In addition Data Transfer Bus control signals are involved in the IACK bus cycle:

1. AS* — the Address Strobe asserted low indicates a valid address is on the bus.
2. DS0* — the lower Data Strobe asserted low indicates a data transfer will occur on bus bits D00–D07.
3. WRITE* — the Read/Write is negated indicating the data is to be read from the Interrupter.
4. A01–A03 — Address lines A01–A03 contain the encoded priority level of the IACK cycle.
5. D00–D07 — Data bus lines D00–D07 are used to pass the interrupt vector from the responding Interrupter to the Interrupt Handler.
6. DTACK* — Data Transfer Acknowledge asserted low signals that the Interrupter has put the vector on the data bus.

FIGURE 5 — SIMPLE VMEbus CONFIGURATION

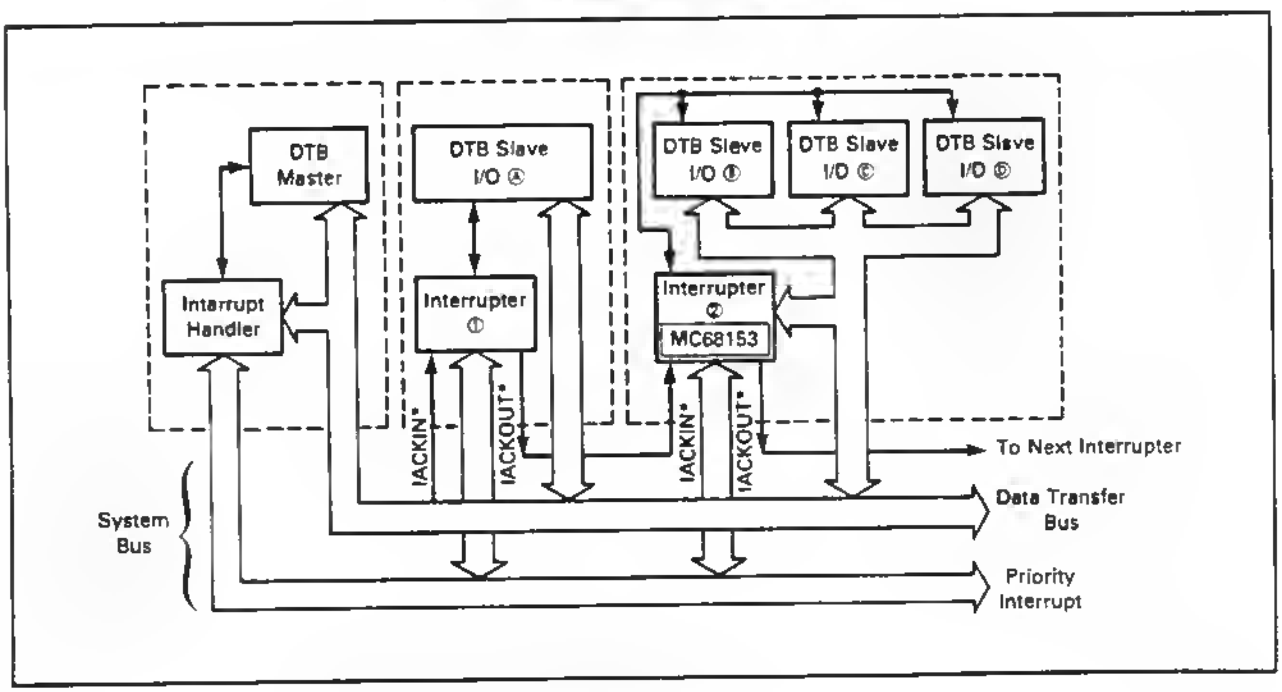
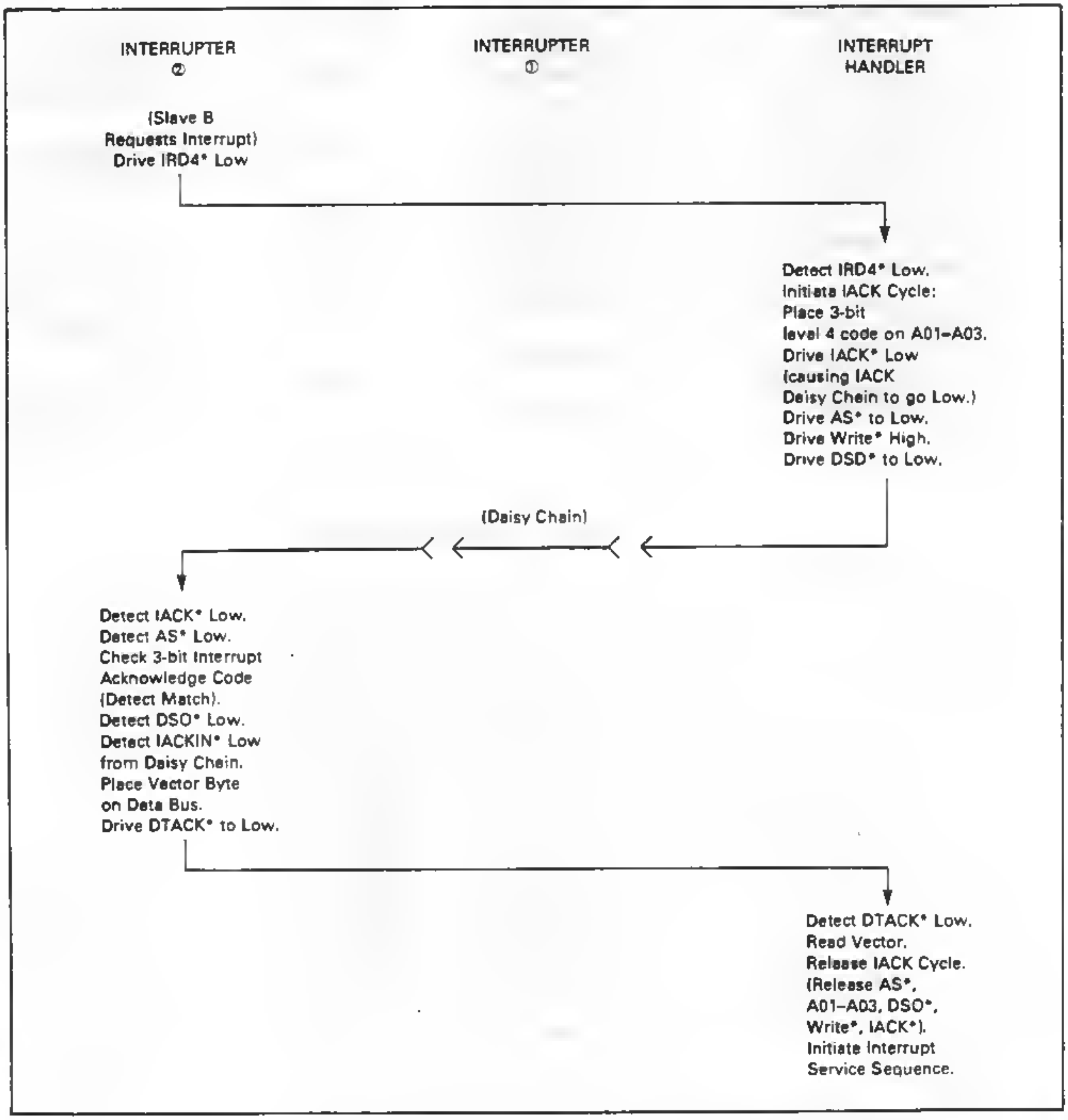


Figure 6 shows a flow diagram of a typical interrupt request and acknowledge operation. Briefly, the sequence of events is first, an Interrupter makes a request, next the Handler responds with an IACK cycle, then the Interrupter passes a vector to the Handler completing the IACK cycle, and finally the Handler uses the vector to determine additional action. Typically, an interrupt service routine is stored in software and the vector determines where its starting address is stored.

Note the daisy chain operation. If the IACK level (on A01–A03) does not match the Interrupter's request level or if no request is pending, the Interrupter passes the IACKIN* signal on and asserts IACKOUT*. This sequential action automatically prioritizes Requesters on the same level (first one in line with a request pending gets serviced) and prevents two or more Interrupters from responding simultaneously.

FIGURE 6 — INTERRUPT REQUEST AND ACKNOWLEDGE OPERATION FLOW DIAGRAM



This discussion is a very cursory look at the bus operation. For more details including situations with multiple bus masters, the user is directed to the VMEbus Specification MVMEBS or VERSAbus Specification M68KVBS. Also, the MC68153 can be used with other buses having similar interrupt structures.

BIM BUS INTERFACE

Figure 7 shows a simplified block diagram of the MC68153 interface to VERSAbus or VMEbus. Address Decode and Control Logic are dependant on the application and must be designed to guarantee BIM ac specifications. It is possible in most cases that the decode logic can be shared with the slave devices. Buffers are provided where shown to comply with bus loading and drive specifications. It is also possible that buffers can be shared with the slave bus interface.

READ/WRITE OPERATION

All eight BIM registers can be accessed from the system bus in both read and write modes. The BIM has an asynchronous bus interface, primarily designed for MC68000-like buses. The following BIM signals generate read and write cycles: Chip Select ($\overline{CS}$), Read/Write (R/$\overline{W}$), Address Inputs (A1–A3), Data Bus (D0–D7), and Data Transfer Acknowledge ($\overline{DTACK}$). During read and write cycles the internal registers are selected by A1, A2, and A3 in compliance with the Figure 4 Truth Table.

Figure 8 shows the device timing for a read cycle. R/$\overline{W}$ and A1–A3 are latched on the falling edge of $\overline{CS}$ and must meet specified setup and hold times. Chip access time for valid data and $\overline{DTACK}$ are dependent on the clock frequency as shown in the figure.

Figure 9 shows the device timing for a write cycle. R/$\overline{W}$, A1–A3, and D0–D7 are latched on the falling edge of $\overline{CS}$ and must meet specified setup and hold times. Chip access time for $\overline{DTACK}$ is dependant on the clock frequency as shown in the figure.

FIGURE 7 — VMEbus/VERSAbus INTERFACE BLOCK DIAGRAM

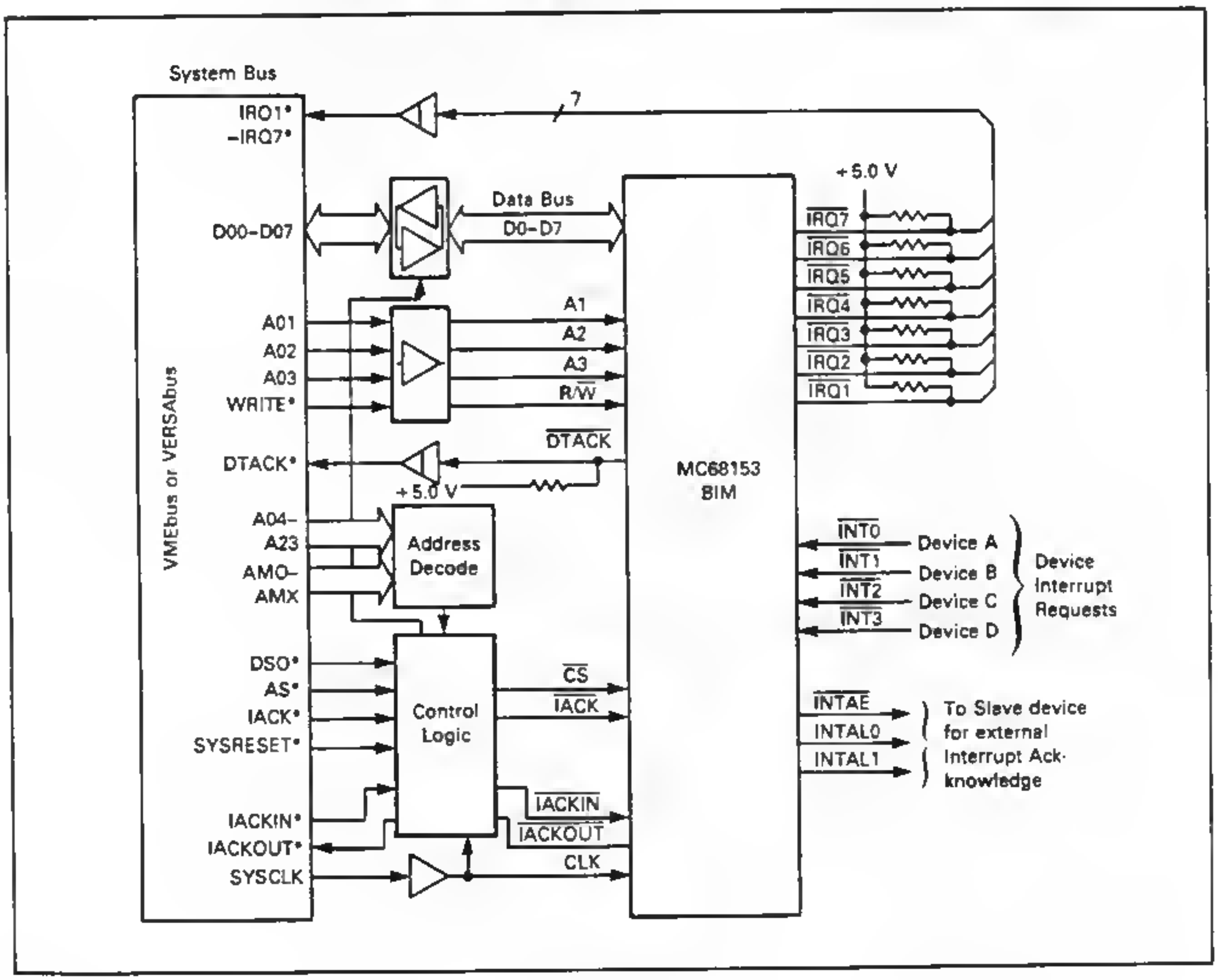


FIGURE 8 — READ CYCLE

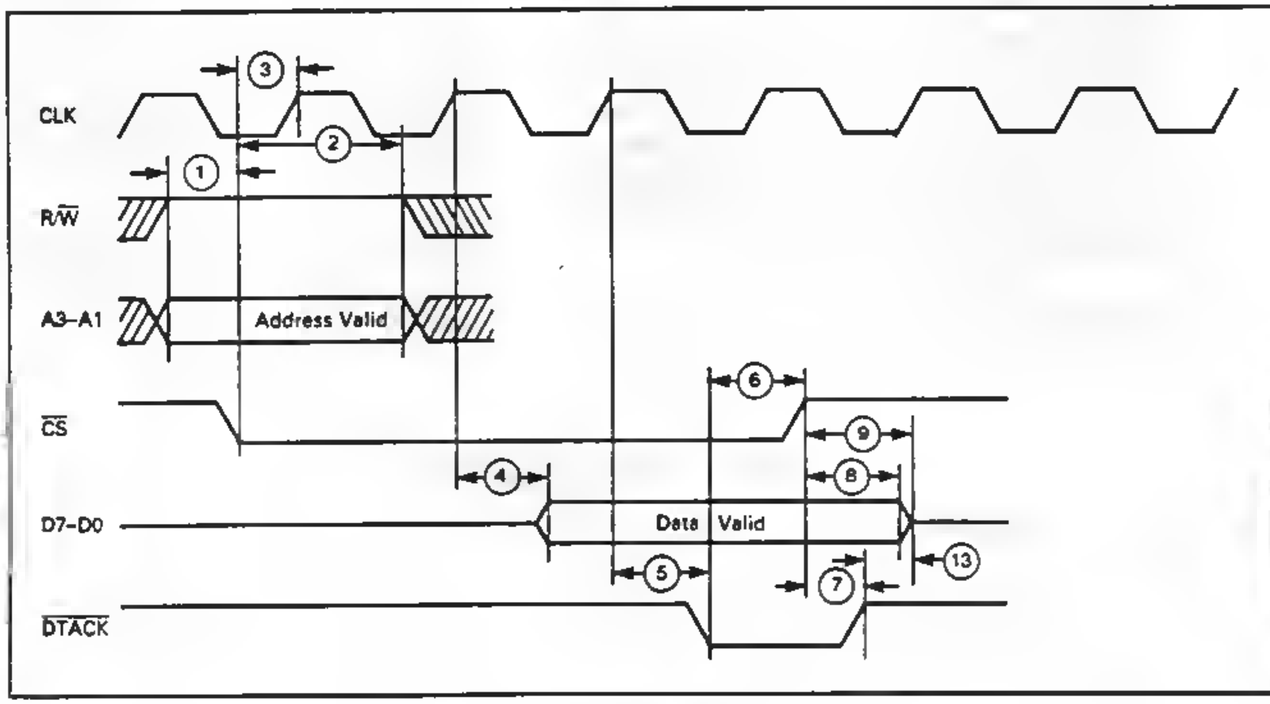
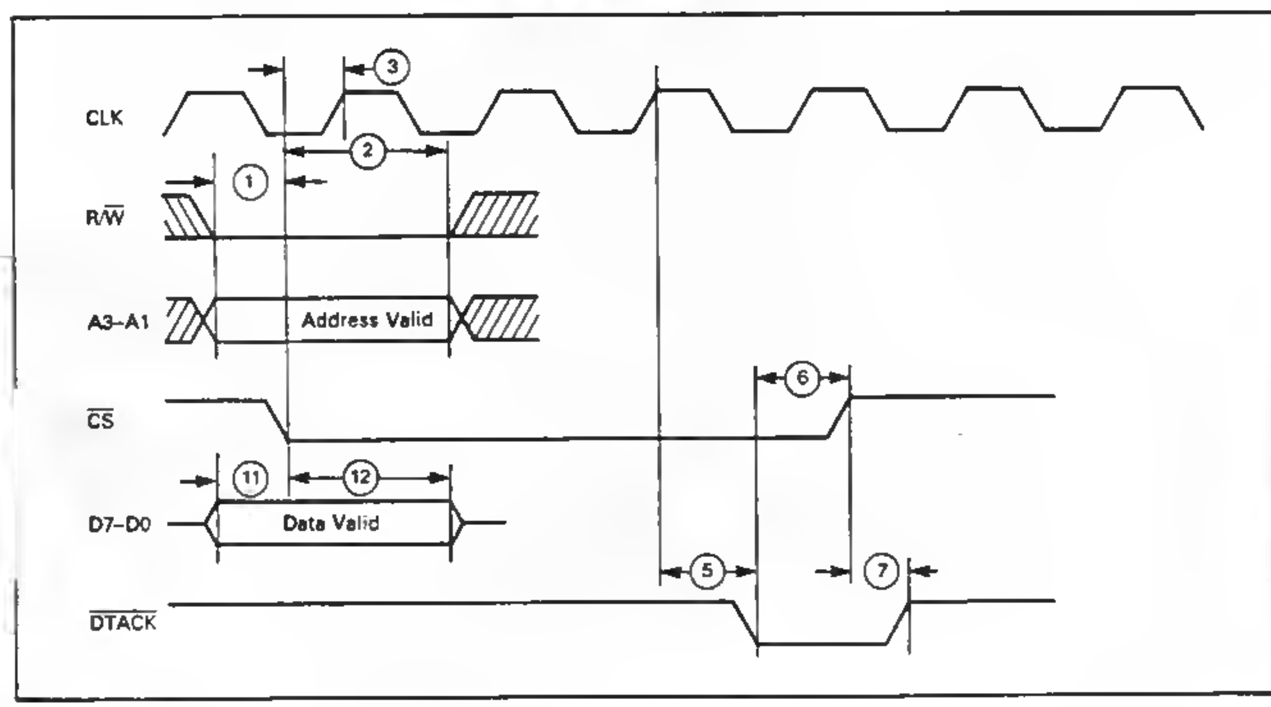


FIGURE 9 — WRITE CYCLE



INTERRUPT REQUESTS

The MC68153 accepts device interrupt requests on inputs $\overline{\mathrm{INT0}}$, $\overline{\mathrm{INT1}}$, $\overline{\mathrm{INT2}}$, and $\overline{\mathrm{INT3}}$. Each input is regulated by Bit 4 (IRE) of the associated control register (CR0 controls $\overline{\mathrm{INT0}}$, CR1 controls $\overline{\mathrm{INT1}}$, etc). If IRE (Interrupt Enable) is set and a device input is asserted, an Interrupt Request open-collector output ($\overline{\mathrm{IRQ1}}$–$\overline{\mathrm{IRQ7}}$) is asserted. The asserted $\overline{\mathrm{IRQX}}$ output is selected by the value programmed in Bits 0, 1, and 2 of the control register (L0, L1, and L2). This 3-bit field determines the interrupt request level as set by software.

Two or more interrupt sources can be programmed to the same request level. The corresponding $\overline{\mathrm{IRQX}}$ output will remain asserted until multiple interrupt acknowledge cycles respond to all requests.

If the interrupt request level is set to zero, the interrupt is disabled because there is no corresponding IRQ output.

INTERRUPT ACKNOWLEDGE

The response of an Interrupt Handler to a bus interrupt request is an interrupt acknowledge cycle. The IACK cycle is initiated in the MC68153 by receiving $\overline{\mathrm{IACK}}$ low. R/$\overline{\mathrm{W}}$, A1, A2, A3 are latched, and the interrupt level on line A1–A3 is compared with any interrupt requests pending in the chip. Further activity can be one of four cases:

1. No further action required — This occurs if $\overline{\mathrm{IACKIN}}$ is not asserted. Asserting $\overline{\mathrm{IACK}}$ only starts the BIM activity. If the daisy chain signal never reaches the MC68153 ($\overline{\mathrm{IACKIN}}$ is not asserted), another Interrupter has responded to the $\overline{\mathrm{IACK}}$ cycle. The cycle will end, the chip $\overline{\mathrm{IACK}}$ is negated, and no additional action is required.

2. Pass on the interrupt acknowledge daisy chain — For this case, $\overline{\mathrm{IACKIN}}$ input is asserted by the preceding daisy chain Interrupter, and $\overline{\mathrm{IACKOUT}}$ output is in turn asserted. The daisy chain signal is passed on when no interrupts are pending on a matching level or when any possible interrupts are disabled. The Interrupt Enable (IRE) bit of a control register can disable any interrupt requests, and in turn, any possible matches.

3. Respond internally — For this case, $\overline{\mathrm{IACKIN}}$ is asserted and a match is found. The MC68153 completes the IACK cycle by supplying an interrupt vector from the proper vector register followed by a $\overline{\mathrm{DTACK}}$ signal asserted. $\overline{\mathrm{IACKOUT}}$ is not asserted because the interrupt acknowledge cycle is completed by this device.

   For the MC68153 to respond in this mode of operation, the EXTERNAL/$\overline{\mathrm{INTERNAL}}$ control register bit (X/$\overline{\mathrm{IN}}$) must be zero. For each source of interrupt request, the associated control register determines the BIM response to an IACK cycle, and the X/$\overline{\mathrm{IN}}$ bit sets this response either internally (X/$\overline{\mathrm{IN}}$ = 0) or externally (X/$\overline{\mathrm{IN}}$ = 1).

4. Respond externally — For the final case, $\overline{\mathrm{IACKIN}}$ is also asserted, a match is found and the associated control register has X/$\overline{\mathrm{IN}}$ bit set to one. The MC68153 does not assert $\overline{\mathrm{IACKOUT}}$ and does assert $\overline{\mathrm{INTAE}}$ low. $\overline{\mathrm{INTAE}}$ signals that the requesting device must complete the IACK cycle (supplying a vector and $\overline{\mathrm{DTACK}}$) and that the 2-bit code contained on outputs INTAL0 and INTAL1 shows which interrupt source is being acknowledged.

These cases are discussed in more detail in the following paragraphs.

Internal Interrupt Acknowledge

For an internal interrupt acknowledge to occur, the following conditions must be met:

1. One or more device interrupt inputs ($\overline{\mathrm{INT0}}$–$\overline{\mathrm{INT3}}$) has been asserted and corresponding control bit IRE value is one.

2. $\overline{\mathrm{IACK}}$ asserted.

3. A match exists between [A3, A2, A1] and the [L2, L1, L0] field of an enabled, requesting control register. If two or more devices are requesting at the same interrupt level, preference is given to the highest number requester, that is, $\overline{\mathrm{INT3}}$ has highest priority and $\overline{\mathrm{INT0}}$ has lowest.

4. Control register bit X/$\overline{\mathrm{IN}}$ of matching interrupt source must be zero.

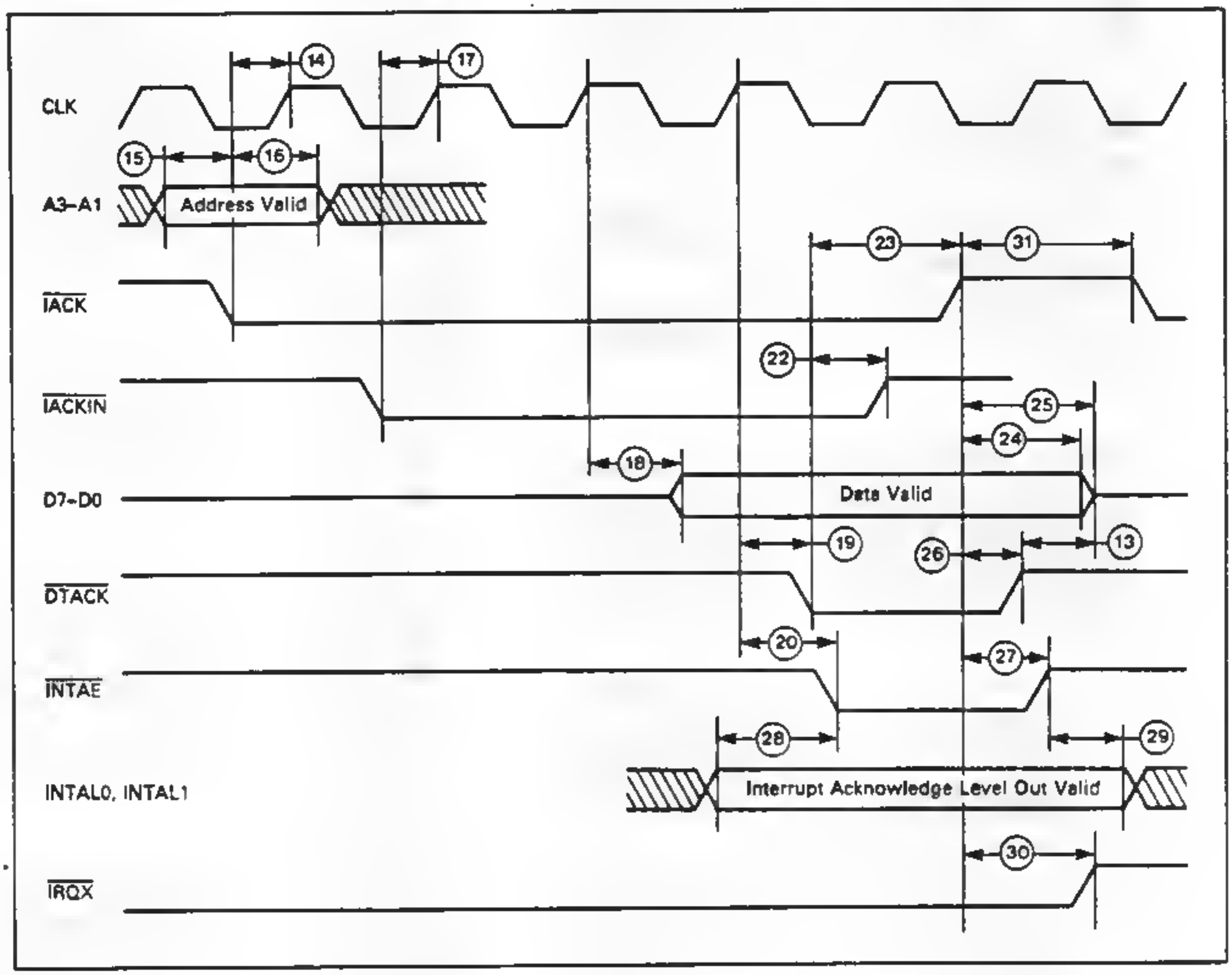
5. $\overline{\mathrm{IACKIN}}$ asserted.

The internal interrupt acknowledge cycle timing is shown in Figure 10. The 8-bit interrupt acknowledge vector is presented to the data bus and $\overline{\mathrm{DTACK}}$ is asserted. Note also that INTAL0 and INTAL1 are valid and $\overline{\mathrm{INTAE}}$ is asserted during this cycle although they would normally not be used. The cycle is terminated (data and $\overline{\mathrm{DTACK}}$ released) after $\overline{\mathrm{IACK}}$ is negated.

During the IACK cycle, the INTERRUPT AUTO-CLEAR control bit (IRAC) comes into play. If the IRAC = one for the responding interrupt source, the INTERRUPT ENABLE (IRE) bit is automatically cleared during the IACK cycle, thus disabling the associated interrupt input and any $\overline{\mathrm{IRQX}}$ output asserted due to this interrupt input. Before another interrupt can be requested from this source, IRE must be set to one by writing to the control register.

Note that $\overline{\mathrm{IACKOUT}}$ is not asserted because this device is responding to the IACK and does not pass the daisy chain signal on. Also, new device interrupt requests occurring on $\overline{\mathrm{INT0}}$–$\overline{\mathrm{INT3}}$ after $\overline{\mathrm{IACK}}$ is asserted are locked out to prevent any race conditions on the daisy chain.

FIGURE 10 — INTERRUPT ACKNOWLEDGE CYCLE — INTERNAL VECTOR



External Interrupt Acknowledge

For an external interrupt acknowledge, the same conditions as listed above are met with one exception. Control register bit X/$\overline{\text{IN}}$ of matching interrupt source must be set to one. The timing is shown in Figure 11. For this cycle, the interrupt vector and $\overline{\text{DTACK}}$ must be supplied by an external device. $\overline{\text{INTAE}}$ is asserted indicating that INTAL0 and INTAL1 are valid. The external device can use these signals to enable the vector and $\overline{\text{DTACK}}$. The cycle is terminated after $\overline{\text{IACK}}$ is negated.

The IRAC control bit acts in the external interrupt acknowledge the same as described for the internal response (see above). Also, $\overline{\text{IACKOUT}}$ is not asserted and new device interrupts are disabled for reasons discussed above.

Pass On IACK Daisy Chain

If the MC68153 has no interrupt request pending at the same level as the interrupt acknowledge, the IACK daisy chain signal is passed on to the next device if $\overline{\text{IACKIN}}$ is asserted. The following conditions are thus met:

1. $\overline{\text{IACK}}$ asserted.
2. No match exists between [A3, A2, A1] and the [L2, L1, L0] field of an enabled, requesting control register.
3. $\overline{\text{IACKIN}}$ is asserted.

$\overline{\text{IACKOUT}}$ is asserted if these conditions are valid. This output drives $\overline{\text{IACKIN}}$ of the next Interrupter on the daisy chain, passing the signal along. Figure 12 shows the timing for this case. $\overline{\text{IACKOUT}}$ is negated after $\overline{\text{IACK}}$ is negated.

FIGURE 11 — INTERRUPT ACKNOWLEDGE CYCLE — EXTERNAL VECTOR

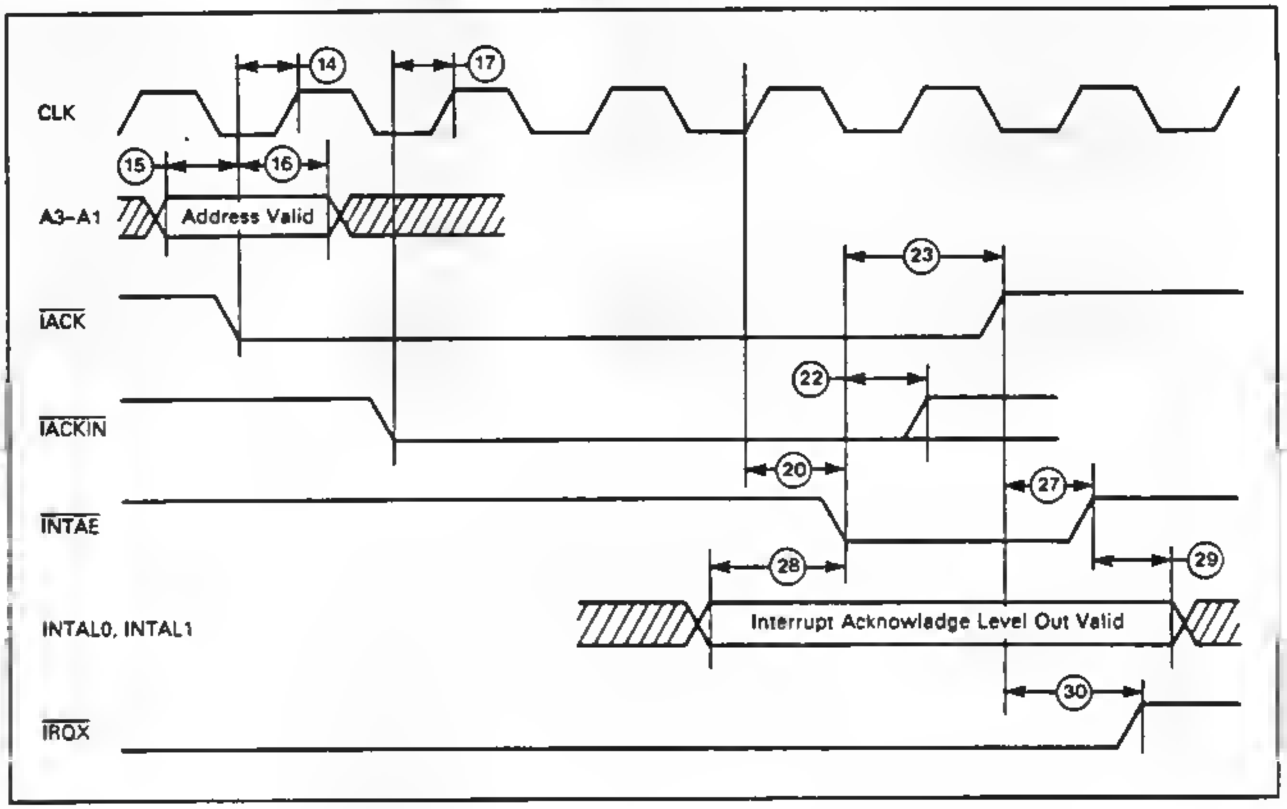
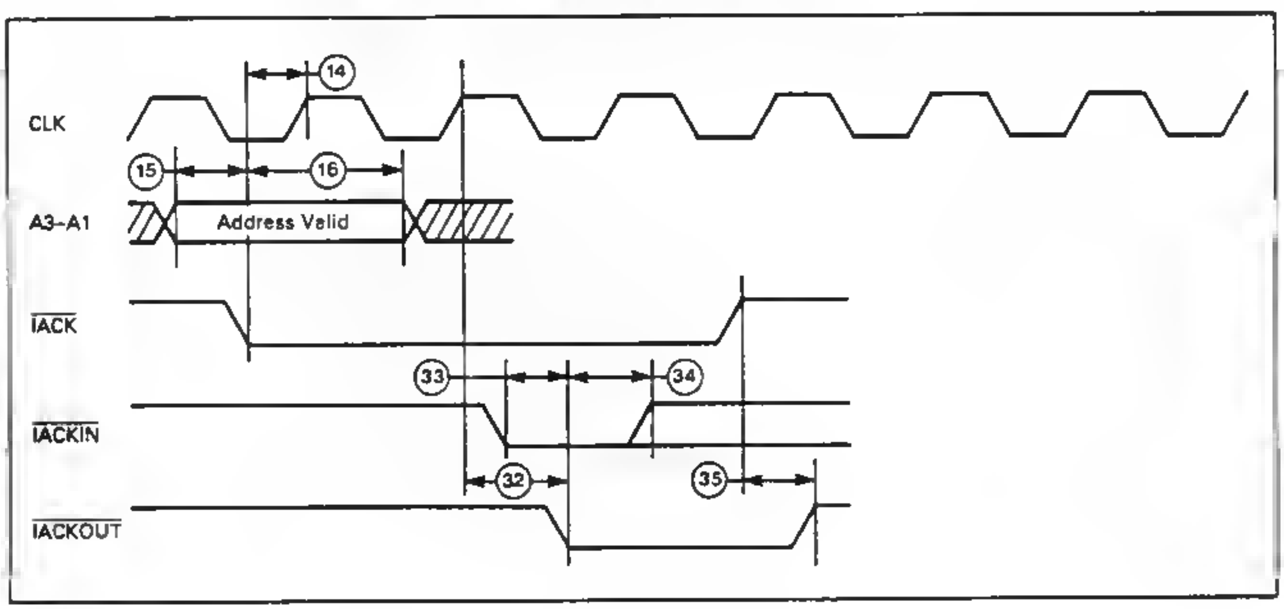


FIGURE 12 — INTERRUPT ACKNOWLEDGE CYCLE — IACKOUT



CONTROL REGISTER FLAGS

Each control register contains a Flag bit (F) and a Flag Auto-Clear bit (FAC). Both bits can be read or altered via a register write without affecting the interrupt operation of the device. The Flag is useful as a status indicator for resource management and as a semaphor in multitasking or multiprocessor systems. Flag (F) is located in bit position 7 and can be used with the MC68000 Test and Set (TAS) instruction.

The Flag Auto-Clear (FAC) is used to manipulate the Flag bit. If the Flag is set to one and the FAC is also one, an interrupt acknowledge cycle to the associated interrupt source clears the Flag bit. This feature is useful in determining the interrupt status and passing messages.

RESET

There is no reset input, however, a chip reset is activated by asserting both $\overline{CS}$ and $\overline{IACK}$ simultaneously (Figure 13). These inputs should be held low for a minimum of two clock cycles for a full reset function. The control registers are reset to all zeroes and the Vector Registers are set to a value of $0F. This vector value is the uninitialized vector for the MC68000. See the MC68000 Users Manual for more details on this vector.

CLOCK

The chip clock is required for internal operation to occur. Typical frequency is 16 MHz in VMEbus and VERSAbus applications derived from the system clock. Any frequency can be used, however, up to 25 MHz (Figure 14).

FIGURE 13 — RESET

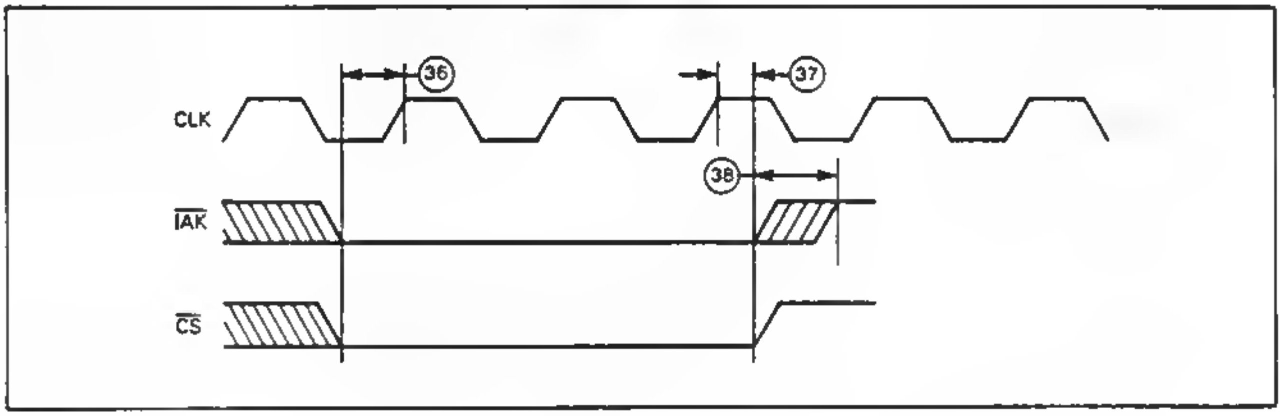


FIGURE 14 — CLOCK WAVEFORM

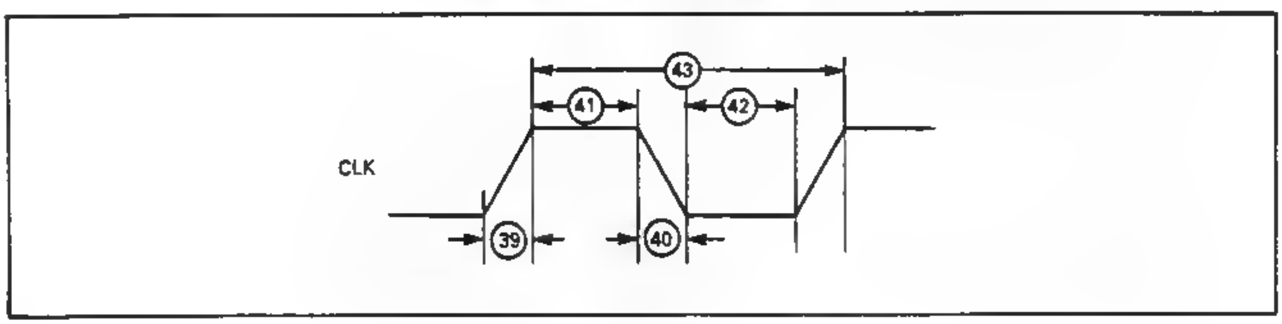


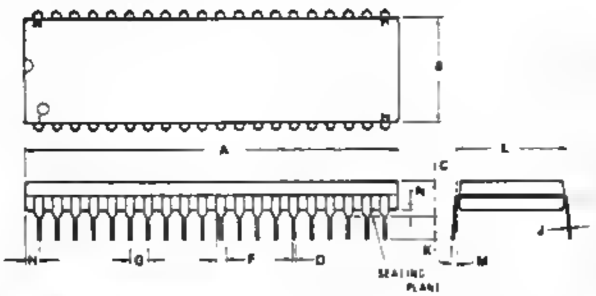
TABLE 1
AC PERFORMANCE SPECIFICATIONS
(V_{CC} = 5.0 V ±5%, T_A = 0°C to 70°C)

Number	Characteristic	Min	Max	Units	Notes
1	R/$\overline{\text{W}}$, A1–A3 Valid to $\overline{\text{CS}}$ Low (Setup Time)	10	—	ns	
2	$\overline{\text{CS}}$ Low to R/$\overline{\text{W}}$, A1–A3 Invalid (Hold Time)	5.0	—	ns	
3	$\overline{\text{CS}}$ Low to CLK High (Setup Time)	15	—	ns	1
4	CLK High to Data Out Valid (Delay)	—	55	ns	2
5	CLK High to $\overline{\text{DTACK}}$ Low (Delay)	—	40	ns	2
6	$\overline{\text{DTACK}}$ Low to $\overline{\text{CS}}$ High	0		ns	
7	$\overline{\text{CS}}$ High to $\overline{\text{DTACK}}$ High (Delay)	—	35	ns	10
8	$\overline{\text{CS}}$ High to Data Out Invalid (Hold Time)	0	—	ns	
9	$\overline{\text{CS}}$ High to Data Out High-Impedance (Hold Time)	—	50	ns	
10	$\overline{\text{CS}}$ High to $\overline{\text{CS}}$ or $\overline{\text{IACK}}$ Low	20	—	ns	
11	Data In Valid to $\overline{\text{CS}}$ Low (Setup Time)	10	—	ns	
12	$\overline{\text{CS}}$ Low to Data In Invalid (Hold Time)	5.0	—	ns	
13	$\overline{\text{DTACK}}$ High to Data Out High-Impedance	—	25	ns	10
14	$\overline{\text{IACK}}$ Low to CLK High (Setup Time)	15	—	ns	1
15	A1–A3 Valid to $\overline{\text{IACK}}$ Low (Setup Time)	10	—	ns	
16	$\overline{\text{IACK}}$ Low to A1–A3 Invalid (Hold Time)	5.0	—	ns	
17	$\overline{\text{IACKIN}}$ Low to CLK High (Setup Time)	15	—	ns	1, 8
18	CLK High to Data Out Valid (Delay)	—	55	ns	3
19	CLK High to $\overline{\text{DTACK}}$ Low (Delay)	—	40	ns	3
20	CLK High to $\overline{\text{INTAE}}$ Low (Delay)	—	40	ns	3
22	$\overline{\text{DTACK}}$ Low to $\overline{\text{IACKIN}}$ High	0	—	ns	8
23	$\overline{\text{DTACK}}$ Low to $\overline{\text{IACK}}$ High	0	—	ns	
24	$\overline{\text{IACK}}$ High to Data Out Invalid (Hold Time)	0	—	ns	
25	$\overline{\text{IACK}}$ High to Data Out High Impedance (Delay)	—	50	ns	
26	$\overline{\text{IACK}}$ High to $\overline{\text{DTACK}}$ High (Delay)	—	45	ns	10
27	$\overline{\text{IACK}}$ High to $\overline{\text{INTAE}}$ High (Delay)	—	35	ns	
28	INTAL0, INTAL1 Valid to $\overline{\text{INTAE}}$ Low (Setup Time)	1.0	2.0	CLK Per	
29	$\overline{\text{INTAE}}$ High to INTAL0, INTAL1 Invalid (Hold Time)	1.0	2.0	CLK Per	
30	$\overline{\text{IACK}}$ High to $\overline{\text{IRQx}}$ High (Delay)	—	50	ns	7, 10
31	$\overline{\text{IACK}}$ High to $\overline{\text{IACK}}$ or $\overline{\text{CS}}$ Low	20	—	ns	
32	CLK High to $\overline{\text{IACKOUT}}$ Low (Delay)	—	40	ns	5
33	$\overline{\text{IACKIN}}$ Low to $\overline{\text{IACKOUT}}$ Low (Delay)	—	30	ns	4, 8
34	$\overline{\text{IACKOUT}}$ Low to $\overline{\text{IACKIN}}$, $\overline{\text{IACK}}$ High	0	—	ns	8
35	$\overline{\text{IACK}}$ High to $\overline{\text{IACKOUT}}$ High (Delay)	—	35	ns	
36	$\overline{\text{IACK}}$ and $\overline{\text{CS}}$ both Low to CLK High (Setup Time)	15	—	ns	9
37	CLK High to $\overline{\text{IACK}}$ or $\overline{\text{CS}}$ High (Hold Time)	0	—	ns	
38	$\overline{\text{IACK}}$ or $\overline{\text{CS}}$ High to $\overline{\text{IACK}}$ and $\overline{\text{CS}}$ High (Skew)	—	1.0	CLK Per	6
39	Clock Rise Time	—	10	ns	
40	Clock Fall Time	—	10	ns	
41	Clock High Time	20	—	ns	
42	Clock Low Time	20	—	ns	
43	Clock Period	40	—	ns	

NOTES:

1. This specification only applies if the VBIM had completed all operations initiated by the previous bus cycle when $\overline{\text{CS}}$ or $\overline{\text{IACK}}$ was asserted. Following a normal bus cycle, all operations are completed within 2 clock cycles after $\overline{\text{CS}}$ or $\overline{\text{IACK}}$ have been negated. If $\overline{\text{IACK}}$ or $\overline{\text{CS}}$ is asserted prior to completion of these operations, the new cycle, and hence, $\overline{\text{DTACK}}$ is postponed.
   If the $\overline{\text{IACK}}$, $\overline{\text{IACKIN}}$ or $\overline{\text{CS}}$ setup time is violated, $\overline{\text{DTACK}}$ may be asserted as shown, or may be asserted one clock cycle later (i.e. $\overline{\text{IACK}}$ will not be recognized until the next rising edge of the clock).
2. Assumes that 3 has been met.
3. Assumes that 14 and 17 have both been met.
4. Assumes that 14 has been met. ($\overline{\text{IACKOUT}}$ cannot go low prior to $\overline{\text{IACKIN}}$ going low).
5. Assumes that 14 has been met and $\overline{\text{IACKIN}}$ has been low for at least the amount of time specified by 33.
6. 38 is the minimum skew between the last moment when both $\overline{\text{IACK}}$ and $\overline{\text{CS}}$ are asserted to when both are negated, to insure that an access cycle is not unintentionally started.
7. Assumes no other $\overline{\text{INTx}}$ input is causing $\overline{\text{IRQx}}$ to be driven low.
8. In non-daisy chain systems, $\overline{\text{IACKIN}}$ may be tied low.
9. Failure to meet this spec. causes RESET to be ignored for 1 clock period. It is then necessary to keep these signals low for 3 clock periods instead of 2.
10. Delay time is specified from Input signal to Open-Collector Output pulled High thru 1.0 kΩ resistor to +5.5 V.

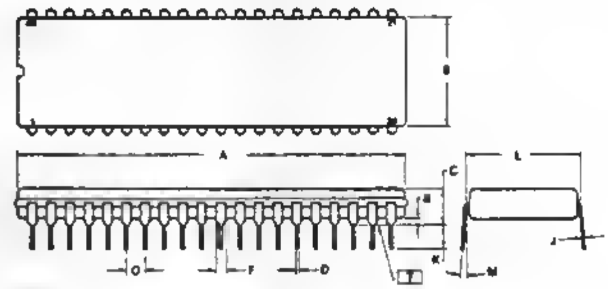
OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.69	52.45	2.035	[illegible]
B	13.72	[illegible]	[illegible]	0.560
C	3.94	5.08	0.155	[illegible]
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

CASE 711-03
PLASTIC PACKAGE



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.31	53.24	2.020	2.096
B	12.70	15.45	0.500	0.610
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

NOTES
1. DIM -A- IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS: ⌖ 0.25(0.010) Ⓜ T A Ⓜ
3. T IS SEATING PLANE.
4. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONS A AND B INCLUDE MENISCUS.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

CASE 734-04
CERAMIC PACKAGE

TYPICAL THERMAL CHARACTERISTICS

Package	θJA (Junction to Ambient) Still Air	Junction Temperature Still Air @ 70°C Ambient
L Suffix	40°C/W	147°C
P Suffix[1]	35°C/W	137°C

NOTES:
1. For reliable system operation the maximum allowable junction temperature (T_J) for plastic encapsulated packages has been limited to +140°C. Exceeding this limit will accellerate "wear-out" mechanisms associated with industry standard assembly methods using thermosonic ball bonds to attach gold (Au) bond wire to aluminum (Al) bond pads on the die surface.
2. At T_J = 140°C, time to 0.1% failure due to Au/Al interconnect = 8,920 Hours.

MOTOROLA *Semiconductor Products Inc.*

BOX 20912 • PHOENIX, ARIZONA 85036 • A SUBSIDIARY OF MOTOROLA INC.

Signetics

SCB68430
Direct Memory Access Interface (DMAI)

Preliminary Specification

Microprocessor Products

DESCRIPTION

The SCB68430 Direct Memory Access Interface (DMAI) is a single channel interface circuit which is intended to complement the performance and architectural capabilities of the SCN68000 microprocessor. The DMAI functions by transferring a series of operands (data) between memory and a device: operand sizes may be byte, word, or long word. A block is a sequence of operands: the number of operands in the block is determined by a transfer count stored within the DMAI. The SCB68430 can be programmed to utilize single cycle (cycle stealing) or burst data transfers.

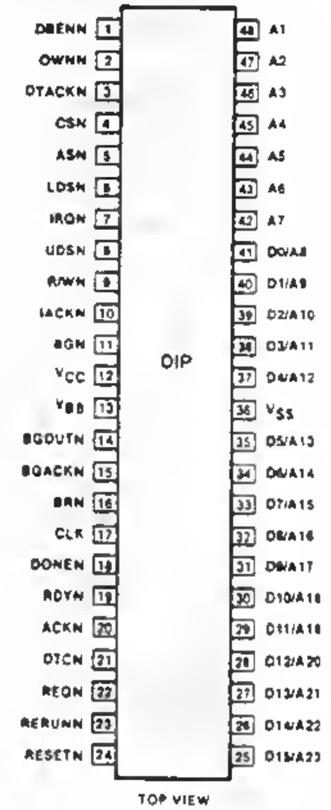
The DMAI provides two interfaces. The microprocessor interface is fully compatible with the SCN68000 microprocessor. The device interface includes lines for requesting, acknowledging, controlling, and timing the data transfers. The DMAI is a single-channel subset of the other 68000 family DMA controllers (68440 and 68450). It is software compatible with these devices and provides similar interfacing signals to both the system bus and the device.

The SCB68430 is constructed using Signetics ISL bipolar technology.

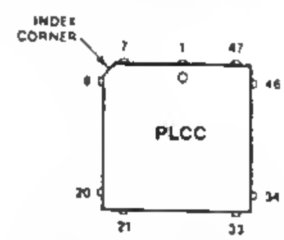
FEATURES

- **Bus compatible with SCN68000 microprocessor**
- **Software compatible with other 68K family DMA controllers**
- **Single address transfers**
- **Cycle steal and burst mode operation**
- **Bus arbitration daisy chain**
- **Automatic rerun on bus error**
- **Supports 32-bit transfers for VME bus**
- **Supports SCN68000 vectored interrupts**
- **24-bit address counter**
- **16-bit transfer counter**
- **Maximum transfer rate of 5 Mbytes per second**
- **Signetics ISL bipolar technology**

PIN CONFIGURATION



CD00450S



CD00052PS

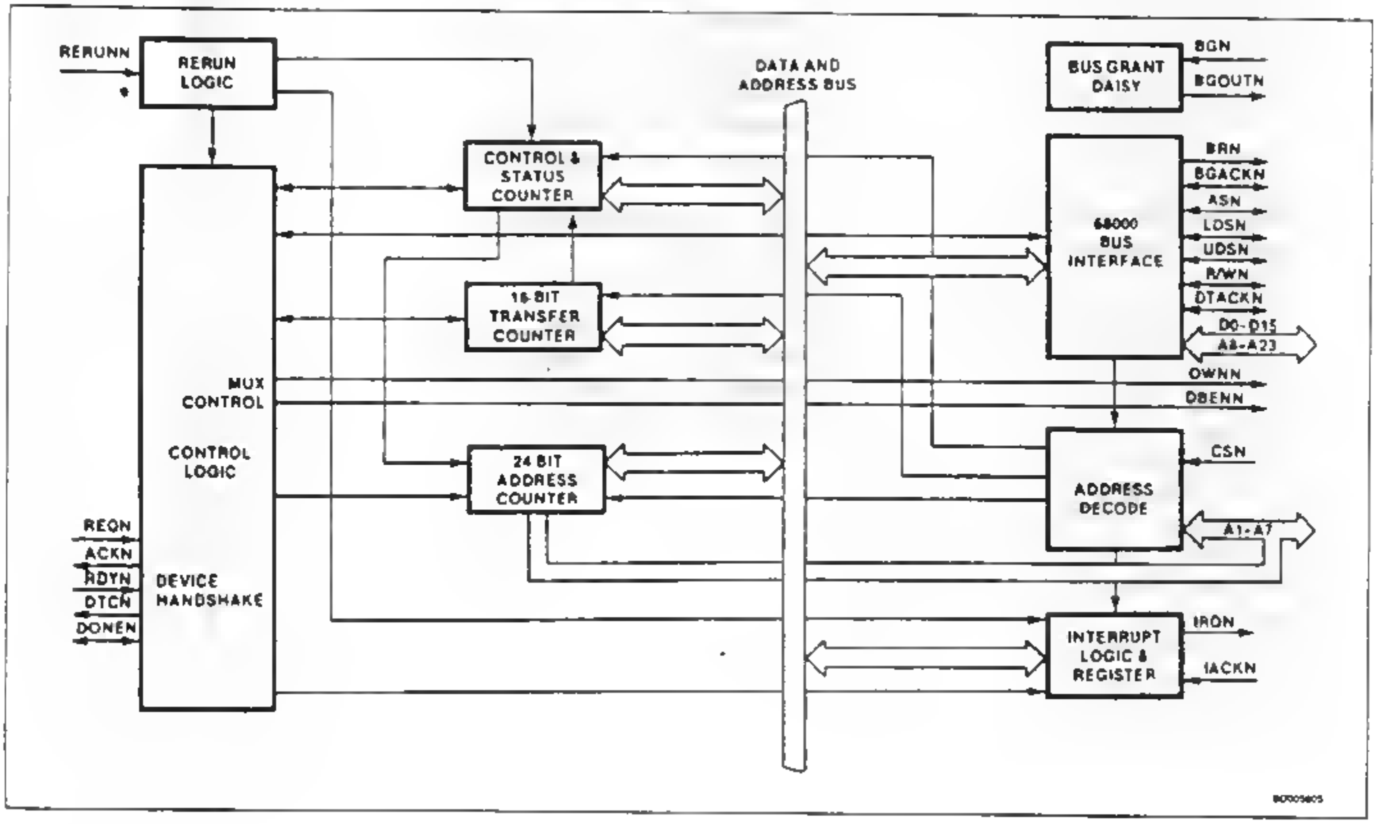
Pin	Function	Pin	Function	Pin	Function
1	NC	19	CLK	36	D7/A15
2	DBENN	20	DONEN	37	D6/A14
3	OWNN	21	RDYN	38	D5/A13
4	DTACKN	22	ACKN	39	V_{SS}
5	CSN	23	DTCN	40	NC
6	ASN	24	REQN	41	D4/A12
7	LDSN	25	RERUNN	42	D3/A11
8	IRQN	26	RESETN	43	D2/A10
9	UDSN	27	NC	44	D1/A9
10	R/WN	28	D15/A23	45	D0/A8
11	IACKN	29	D14/A22	46	A7
12	BGN	30	D13/A21	47	A6
13	V_{CC}	31	D12/A20	48	A5
14	NC	32	D11/A19	49	A4
15	V_{BB}	33	D10/A18	50	A3
16	BGOUTN	34	D9/A17	51	A2
17	BGACKN	35	D8/A16	52	A1
18	BRN				

Direct Memory Access Interface (DMAI) SCB68430

ORDERING CODE

PACKAGES	V_{CC} = 5V ± 5%, T_A = 0°C to 70°C	
	10MHz	12.5MHz
Ceramic DIP	SCB68430CAI48	SCB68430CCI48
Plastic DIP	SCB68430CAN48	SCB68430CCN48
Plastic LCC	SCB68430CAA52	SCB68430CCA52

BLOCK DIAGRAM



Direct Memory Access Interface (DMAI) SCB68430

PIN DESCRIPTION

MNEMONIC	PIN NO.	TYPE	DESCRIPTION
A1 – A7	48 – 42	I/O	**Address Lines:** Active high, three-state. In the MPU mode, these low order address lines specify which internal register of the DMAI is being accessed. In DMA mode, A1 – A7 are ouputs which provide the low order address bits of the location being accessed. Three-stated in IDLE Mode.
A8 – A23/ D0 – D15	41 – 37 35 – 25	I/O	**Address/Data Lines:** Active high, three-state. These lines are time multiplexed for data and address leads. The lines OWNN, RWN, CSN, and DBENN are used to control the demultiplexing of the address and data using external circuitry. In MPU mode, the bidirectional data lines (D0 – D15) are used to transfer data between the MPU and the DMAI. In the DMA mode, A8 – A23 provide the high order address bits of the location being accessed. Three-stated in IDLE mode.
ASN	5	I/O	**Address Strobe:** Active low, three-state. In MPU and IDLE modes, ASN is an input which indicates that the current bus master has placed a valid address on the bus. It is monitored by the DMAI during bus arbitration to ascertain that the previous bus master has completed the current bus cycle. In DMA mode, it is an output indicating that the DMAI has placed a valid address on the bus.
UDSN	8	I/O	**Upper Data Stobe:** Active low, three-state. In MPU and IDLE modes, UDSN is an input which indicates that the upper data byte of the addressed word is being addressed. In DMA mode, it is an output with the same meaning.
LDSN	6	I/O	**Lower Data Strobe:** Active low, three-state. In MPU and IDLE modes, LDSN is an input which indicates that the lower data byte of the addressed word is being addressed. In DMA mode, it is an output with the same meaning.
R/WN	9	I/O	**Read/Write:** Active high for read, low for write, three-state. In MPU mode, R/WN is an input which controls the direction of data flow through the DMAI's input/output data bus interface and, if required, through an external data bus buffer. R/WN high causes the DMAI to place the data from the addressed register on the data bus, while R/WN low causes the DMAI to accept data from the data bus. In DMA mode, R/WN is an output to memory and I/O controllers indicating the type of bus cycle. It is held three-stated during IDLE mode.
CSN	4	I	**Chip Select:** Active low. When low, places the DMAI into the MPU mode. This input signal is used to select the DMAI for programmed data transfers. These transfers take place over D0 – D15 as controlled by the R/WN and A1 – A7 inputs. The DMAI is deselected when CSN is high. CSN is ignored during DMA mode.
DTACKN	3	I/O	**Data Transfer Acknowledge:** Active low, three-state. In MPU mode, DTACKN is asserted on a write cycle to indicate that the data on the bus has been latched, and on a read cycle or interrupt acknowledge cycle to indicate that valid data is present on the bus. The signal is negated (driven high) when completion of the cycle is indicated by negation of the CSN or IACKN input, and returns to the inactive third state a short time after it is negated. In DMA Mode, DTACKN is an input monitored by the DMAI to determine when the addressed device (memory) has latched the data (write cycle) or put valid data on the bus (read cycle).
RESETN	24	I	**Master Reset:** Active low. Assertion of this pin clears internal control registers (See table 1), initializes the interrupt vector register to H'0F', and sets the status register to the default value B'0000 000X', where X is the state of RDYN. All bidirectional I/O lines are three-stated and the DMAI is placed in the IDLE mode.
CLK	17	I	**Clock:** Active high. Usually the system clock, but may be any clock meeting the electrical specifications. Used by the DMAI to synchronize device functions and external control lines, and may not be gated off at any time.
IRQN	7	O	**Interrupt Request:** Active low, open collector. This output is asserted, if interrupts are enabled, upon end of transfer, on occurrence of a bus error, and on receipt of an abort from the MPU. The CPU can read the status register to determine the interrupting condition(s), or can respond with an interrupt acknowledge cycle to cause the DMAI to output an interrupt vector on the data bus.
IACKN	10	I	**Interrupt Acknowledge:** Active low. When asserted, indicates that the current cycle is an interrupt acknowledge cycle. The DMAI normally responds by placing the contents of the interrupt vector register on the data bus and asserting DTACKN. IACKN is not serviced if the DMAI has not generated an interrupt request.
BRN	16	O	**Bus Request:** Active low, open collector. BRN is asserted by the DMAI to request ownership of the bus after a DMA request is sensed on the REQN input from the I/O device. It is negated when the bus has been granted (BGN low) and BGACKN has been asserted, or, in burst DMA request mode, if the I/O device negates its request at least one clock cycle before BGACKN is asserted.
BGN	11	I	**Bus Grant:** Active low. BGN indicates to the DMAI that it is to be the next bus master. This signal is originated by the MPU and propagated via a daisy chain or other prioritization mechanism. After BGN is asserted, the DMAI waits until DTACKN, ASN, and BGACKN have become inactive before assuming ownership of the bus by asserting BGACKN.

PIN DESCRIPTION (Continued)

MNEMONIC	PIN NO.	TYPE	DESCRIPTION
BGOUTN	14	O	**Bus Grant Output:** Active low. Daisy chain output which is asserted by the DMAI when BGN is asserted and the DMAI does not have a bus request pending.
BGACKN	15	I/O	**Bus Grant Acknowledge:** Active low, three-state. As an input, BGACKN is monitored by the DMAI during the bus arbitration cycle to determine when it can assume ownership of the bus (BGACKN negated). In DMA mode, it is asserted by the DMAI to indicate that it is the bus master. Three-stated in MPU and IDLE modes.
RERUNN	23	I	**Rerun:** Active low. This input is asserted by external error detect logic to indicate a bus error. In DMA mode, the DMAI stops operation and three-states the data, address, and control lines, except BGACKN. It remains halted until RERUNN becomes inactive, and then re-tries the last bus cycle. If RERUNN is asserted again, the DMAI sets the ERR bit in the status register, stops DMA operation, releases the bus, and interrupts the CPU, if interrupts are enabled, responding with a special interrupt vector when IACKN is asserted. Not monitored in MPU and IDLE modes.
REQN	22	I	**DMA Request:** Active low. This input from the I/O device requests service from the DMAI and causes the DMAI to request control of the bus. In burst mode, the input is level sensitive, and the DMAI releases the bus after REQN is negated and the current DMA cycle is completed. In cycle steal mode, the REQN input is negative edge triggered. A negative going edge must occur at least one clock cycle before DTCN is asserted to accomplish continuous transfer cycles but not earlier than beginning of master cycle.
ACKN	20	O	**DMA Request Acknowledge:** Active low. ACKN is asserted by the DMAI to indicate that it has gained the bus and the requested bus cycle is now beginning. It is asserted at the beginning of every bus cycle after ASN has been asserted, and is negated at the end of every bus cycle.
RDYN	19	I	**Device Ready:** Active low. RDYN is asserted by the requesting device to indicate to the DMAI that valid data has either been stored or put on the bus. If negated, it indicates that the data has not been stored or presented, causing the DMAI to enter wait states. RDYN can be held low continuously if the device is fast enough so that wait states are not required.
DTCN	21	O	**Device Transfer Complete:** Active low. In DMA mode, DTCN is asserted by the DMAI to indicate to the device that the requested data transfer is complete. On a write to memory operation, it indicates that the data provided by the device has been successfully stored. On a read from memory operation, it indicates to the device that the data from memory is present on the data bus and should be latched.
DONEN	18	I/O	**Done:** Active low, open collector. As an output, DONEN is asserted by the DMAI concurrent with the ACKN output to indicate to the device that the transfer count is exhausted and that the DMAI's operation is completed as a result of that transfer. As an input, if asserted by the device before the transfer count became zero, it causes the DMAI to abort service and generate an interrupt request, if interrupts are enabled.
OWNN	2	O	**Own:** Active low, open collector. This output is asserted by DMAI during the DMA mode to indicate bus mastership. It can be used to enable external address/data and control buffers. Inactive in MPU and IDLE modes.
DBENN	1	O	**Data Bus Enable:** Active low, open collector. Asserted by the DMAI when CSN is asserted or when IACKN is asserted and the DMAI has an interrupt request pending. Can be used to enable bidirectional data buffers for D0 – D15. Inactive in IDLE and DMA mode.
V_{CC}	12	I	**Power Supply:** +5 volt power input.
V_{BB}	13	I	**Power Supply:** +1.5 volt power input.
V_{SS}	36	I	**Ground:** Signal and power ground input.

PIN DESCRIPTION

The Pin Description table describes the function of each of the pins of the DMAI. Signal names ending in 'N' are active low. All other signals are active high. In the descriptions, 'MPU mode' refers to the state when the DMAI is chip selected. The term 'DMA mode' refers to the state when the DMAI assumes ownership of the bus. The DMAI is in the 'IDLE' mode' at all other times.

In this data sheet signals are discussed using the terms 'active' and 'inactive' or 'asserted' and 'negated' independent of whether the signal is active in the high (logic one) state or the low (logic zero) state. Refer to the individual pin descriptions for the definition of the active level of each signal.

REGISTERS AND COUNTERS

Register Map

The internal accessible register organization of the DMAI is shown in table 1. The following rules apply to all registers:

1. A read from a reserved location in the map results in a read from the 'null register'. The null register returns all ones for data and results in a normal bus cycle. A write to one of these locations results in a normal bus cycle but no write occurs.
2. Unused bits of a defined register are read as indicated in the register descriptions.
3. All registers are addressable as 8-bit quantities. To facilitate operation with the 68K MOVEP instruction, addresses are ordered such that certain sets of registers may also be accessed as words or long words.

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The operation of the DMAI is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The contents of certain control and status registers are initialized on RESET.

To provide compatibility with the other 68K family DMA controllers, control and status bits are mapped in bit positions equivalent to where they are located in the register map of the other devices. Bits which are used in the other devices but not in the DMAI are assigned default values. If upward compatibility to the other controllers is required, the programmer should use these default values when writing the control words to the registers, although they have no effect in the DMAI. When a register is read, the default value is returned regardless of the value used when the register is programmed. The default value is indicated by '(x)' in unused bit positions in the register formats, which are illustrated in table 2.

Table 1. DMAI ADDRESS MAP

ADDRESS BITS[1,2] 7 6 5 4 3 2 1 0	ACRONYM	REGISTER NAME	MODE	AFFECTED BY RESET
d d 0 0 0 0 0 0	CSR	Channel Status Register	R/W[3]	Yes
d d 0 0 0 0 0 1	CER	Channel Error Register	R	Yes
d d 0 0 0 0 1 0		Reserved		
d d 0 0 0 0 1 1		Reserved		
d d 0 0 0 1 0 0	DCR	Device Control Register	R/W	Yes
d d 0 0 0 1 0 1	OCR	Operation Control Register	R/W	Yes
d d 0 0 0 1 1 0	SCR	Sequence Control Register	R/W[4]	No
d d 0 0 0 1 1 1	CCR	Channel Control Register	R/W	Yes
d d 0 0 1 0 0 0		Reserved		
d d 0 0 1 0 0 1		Reserved		
d d 0 0 1 0 1 0	MTCH	Memory Transfer Counter High	R/W	No
d d 0 0 1 0 1 1	MTCL	Memory Transfer Counter Low	R/W	No
d d 0 0 1 1 0 0	MACH	Memory Address Counter High	R/W[4]	No
d d 0 0 1 1 0 1	MACMH	Memory Address Counter Middle High	R/W	No
d d 0 0 1 1 1 0	MACML	Memory Address Counter Middle Low	R/W	No
d d 0 0 1 1 1 1	MACL	Memory Address Counter Low	R/W	No
d d 0 1 d d d d		Reserved		
d d 1 0 0 0 d d		Reserved		
d d 1 0 0 1 0 0		Reserved		
d d 1 0 0 1 0 1	IVR	Interrupt Vector Register – Normal	R/W	Yes
d d 1 0 0 1 1 0		Reserved		
d d 1 0 0 1 1 1	IVR	Interrupt Vector Register – Error	R/W	Yes
d d 1 0 1 0 d d		Reserved		
d d 1 0 1 1 0 0		Reserved		
d d 1 0 1 1 0 1	CPR	Channel Priority Register	R/W[4]	No
d d 1 0 1 1 1 0		Reserved		
d d 1 0 1 1 1 1		Reserved		
d d 1 1 d d d d		Reserved		

NOTES:
1. A0 = 0 for UDSN asserted, A0 = 1 for LDSN asserted.
2. 'd' designates don't care.
3. A write to this register may perform a status resetting operation.
4. This register is a dummy register present only to provide compatibility with other 68K family DMA controllers. A write to this register has no effect on the DMAI.

Table 2. REGISTER BIT FORMATS

DEVICE CONTROL REGISTER

	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT09	BIT08
DCR	EXTERNAL REQUEST MODE 0 = BURST 1 = CYCLE STEAL	NOT USED (0)	NOT USED (1)	NOT USED (1)	NOT USED (*)	NOT USED (0)	NOT USED (0)	NOT USED (0)

*Should be programmed as '0' for SIZE (OCR[5:4]) = 00 and as '1' otherwise. When read, the value of this bit is OCR[5]. .OR.OCR[4].

2

OPERATION CONTROL REGISTER (OCR)

	BIT07	BIT06	BIT05	BIT04	BIT03	BIT02	BIT01	BIT00
	DIRECTION		OPERAND SIZE					
OCR	0 = MEM TO DEV 1 = DEV TO MEM	NOT USED (0)	00 = BYTE 01 = WORD (16 BIT) 10 = LONG WORD* 11 = WORD (32-BIT)*		NOT USED (0)	NOT USED (0)	NOT USED (1)	NOT USED (0)

*Long word and 32-bit word modes are not supported by 68440. 32-bit word mode is not supported by 68450.

SEQUENCE CONTROL REGISTER (SCR)

	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT09	BIT08
SCR	NOT USED (0)	NOT USED (0)	NOT USED (0)	NOT USED (0)	NOT USED (0)	NOT USED (1)	NOT USED (0)	NOT USED (0)

CHANNEL CONTROL REGISTER (CCR)

	BIT07	BIT06	BIT05	BIT04	BIT03	BIT02	BIT01	BIT00
	START			SOFTWARE ABORT	INTERRUPT ENABLE			
CCR	0 = NO 1 = YES	NOT USED (0)	NOT USED (0)	0 = NO 1 = YES	0 = NO 1 = YES	NOT USED (0)	NOT USED (0)	NOT USED (0)

CHANNEL STATUS REGISTER (CSR)

	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT09	BIT08
	CHANNEL OPERATION COMPLETE		NORMAL DEVICE TERMINATE	ERROR	CHANNEL ACTIVE			READY INPUT STATE
CSR	0 = NO 1 = YES	NOT USED (0)	0 = NO 1 = YES	0 = NO 1 = YES	0 = NO 1 = YES	NOT USED (0)	NOT USED (0)	0 = LOW 1 = HIGH

CHANNEL ERROR REGISTER (CER)

	BIT07	BIT06	BIT05	BIT04	BIT03	BIT02	BIT01	BIT00
				ERROR CODE				
CER	NOT USED (0)	NOT USED (0)	NOT USED (0)	00000 = NO ERROR 01001 = BUS ERROR 10001 = SOFTWARE ABORT				

CHANNEL PRIORITY REGISTER (CPR)

	BIT07	BIT06	BIT05	BIT04	BIT03	BIT02	BIT01	BIT00
CPR	NOT USED (0)	NOT USED (0)	NOT USED (0)	NOT USED (0)	NOT USED (0)	NOT USED (0)	NOT USED (0)	NOT USED (0)

Device Control Register (DCR)

[15] External Request Mode

This bit selects whether the DMAI operates in burst or cycle steal mode.

0 Burst mode. This mode allows a device to request the transfer of multiple operands using consecutive bus cycles. In this mode the request (REQN) line is an active low input which is asserted by the device to request an operand transfer. The DMAI services the request by arbitrating for the bus, obtaining the bus, and notifying the peripheral by asserting the acknowledge (ACKN) output. If the request line is active when the DMAI asserts ACKN, and remains active at least until the DMAI asserts device transfer complete (DTCN), the DMAI recognizes a valid request for another operand, which will be transferred during the next bus cycle. If the request line is negated before the DMAI asserts DTCN, the DMAI relinquishes the bus and waits for the next request, but the current transfer will be completed.

1 Cycle steal mode. In this mode, the device requests an operand transfer by generating a falling edge on the request (REQN) line. The DMAI services the request by arbitrating for the bus, obtaining the bus, and notifying the peripheral by asserting the acknowledge (ACKN)

output. The request line must be in the inective stale for at least one clock cycle before a request is made. After e request has been asserted, it must remain et the assertion level for al least one clock cycle. If another requesl is received before the firsl operend part of a former request is acknowledged, the second request is not recognized. Normally, the DMAI will relinquish the bus after servicing a valid request. However, il the device generates a new request before the DMAI asserts DTCN for the fast operand part, the DMAI will relain ownership of the bus and that request will be serviced before the bus is relinquished.

Operation Control Register (OCR)

[7] Direction

0 Transler is from momory to device.

1 Transler is Irom device to memory.

[5:4] Operand Size

The programming ol these bits determine whether UDSN, LDSN, or both are generated during Ihe Iransfer cycle and the increment by which Ihe membry address counler (MAC) is changed in each transler cycle.

00 Byte. The operand size is 8 bits. The MAC is incremented by one after each operand Iransler. If the LSB of the MAC is a '0', UDSN is asserted during the transfer. Il the LSB ol a MAC is e '1', LDSN is asserted during Ihe Iransler. The transfer counler decrements by one betore each byte is transferred.

01 Word. The operand size is 16 bits. The MAC is incremenled by Iwb after each operand transler. The value ol the LSB ol the MAC is ignored and both UDSN and LDSN are asserted during the transfer. The transfer counler decrements by one before each word is translerred.

10 Long word. The operand size is 32 bits. The operand is transferred as two 16-bit words. The MAC is incremenled by two after each 16-bit word is transferred. The value of the LSB of the MAC is ignored and both UDSN and LDSN are esserted during the transler. The transler counter decrements by one before the enlire long word is transferred. Note that this mode is not implemented in the 68440.

11 Double word. The operand size is 32 bits. The operand is lransferred as a single 32-bit word. The MAC is incremenled by four efter each operand transfer. The velue ol the two LSBs ol the MAC is ignored (Ihe A1 output will always be a zero in this mode) end both UDSN end LDSN are asserted during the transler. The transler counter decrements by one beloie the double word is translerred. Note that this mode is not implemented in the 68440 or 68450; it is included in the DMAI to support VME bus operations.

Sequence Control Register (SCR)

This regisler serves no funclion in the DMAI. Il is included only to provide compatibilily with the programming for the 68440 and 68450 DMA conlrollers.

Channel Control Register (CCR)

[7] Start Operation

0 No start pending.

1 Start operation. The start bil is set to initiate operation of the DMAI. The memory address counter and the memory transfer counter should have been previously initialized, and all bits of the channel status register (CSR) should have previously been reset. The DMAI initiates operation by clearing any pending requests, clearing the start bit, and setting the channel active bit in the CSR. The DMAI is then ready to receive requests for an operation. The channel cannot be started if any of the internal slalus bits in the CSR (CSR[15:11]) have nol been cleared.
A pending stert cannbt be reset by a write to the register. START can be cleared only by the DMAI when it starts operalion or by setting the softwere abort bit (CCR[4]).

[4] Software Abort

0 Do not abort.

1 Abort operation. Setting this bit terminates the current operation of Ihe DMAI and places it in the IDLE state. The channel operetion complete end error bits in the CSR are set, the channel active bil in the CSR is reset, and an ABORT ERROR condition is signaled in the CER. Setting this bit causes a pending start to be resel.

[3] Interrupt Enable

0 Interrupts not enabled.

1 Enable interrupts. An inlerrupt requesl is generated if the channel operelion complete bit in the CSR is sel. When the IACKN input is asserted, the DMAI returns the normal interrupt vector if the error bit in the CSR is not set, or the error interrupt vector it error is set.

Channel Status Register (CSR)

A read of this register provides the status of the DMAI. The COC, NDT, and ERR bits can be cleared by writing a '1' to the bit positions of the register which are lo be cleared. Those bit positions which are written with a '0' remain unaffected.

[15] Channel Operation Complete

This bit is set following the termination, whether successful or not, of any DMAI operation and indicates that the DMA transfer has completed. This bit must be cleared to start another channel operation.

[13] Normal Device Termination

This bit is set when the device terminates the DMAI operetion by asserting Ihe DONEN line while the device was being acknowledged. This bit must be cleared to start another channel operation.

[12] Error

This bil is used to report that the DMAI's operation was terminated due to the occurrence ol an error. The condition which caused the error can be delermined by reading Ihe chennel error regisler (CER). This bil must be cleared to start anolher channel operation. When this bil is cleared, the CER is also cleared.

[11] Channel Active

This bit is set aller the chennel has been started and remains sel until the chennel operation terminates. It is Ihen automatically cleared by the DMAI. The bit is unaffecled by the write operalions.

[8] Ready Input State

This bit rellects the state of the RDYN input at the time the CSR is reed. The bil is a '0' it RDYN is low and a '1' if RDYN is high. This bit is unaffected by write or resel operations.

Channel Error Register (CER)

[4:0] Error Code

This field indicates the source of error when en error is indicaled in CER[12]. The contents ol this register are cleared when CER[12] is cleared

00000 No error

01001 Bus error. A bus error occurred during the last bus cycle generated by the DMAI. See rerun description in OPERATION section.

10001 Software abort. The channel operation wes terminated by a software ebort commend. See CCR[4].

Channel Priority Register (CPR)

This register serves no function in the DMAI. It is included only to provide compalibility with the programming for the other 68K family DMA controllers.

Memory Address Counter (MACH, MACMH, MACML, MACL)

The 32-bit memory address counler is used lo program Ihe memory location where the first operand lo be Iransferred is located or is to be transferred to, depending on the direction ot Iransler. The counter must be initialized prior to beginning the transfer ol a block ol data and then increments automatically depending on the operand length, as de-

scribad in the Operation Control Register description.

Only the least significant 24 bits of the counter (MACMH, MACML, and MACL) are implemented in the DMAI. The most significant byte of tha counter, MACH, is provided only to allow compatibility with programming of the 68440 and 68450. Writing to MACH has no elfect on the DMAI operation. Raading MACH always raturns H'00'.

Memory Transfer Counter (MTCH, MTCL)

The 16-bit mamory transfer counter programs the number ol operands to be transferred by the DMAI. The counter must be initialized prior to beginning the transfer of a block ol data and than decraments onca par operand transfer (regardless of operand size) until it raaches the terminal value of zero. Channel operation then terminatas and the COC bit in the CSR will be asserted.

Interrupt Vector Register (IVR)

The IVR contains the value to be placed on the data bus upon receipt of an interrupt acknowledge from the MPU. Only the saven most significant bits of the programmed value are used by the DMAI. The output vector from the DMAI contains a zero in the least significant bit position if a normal termination occurred (airor bit not sat) and contains a ona in the least significant bit position if termination was due to an error (error bit set).

The contents of this register are initialized to H'0F' by a reset. The value returned will be H'0F', ragardless of the arroi state, until the ragistar is programmed by tha MPU.

To provide compatibility with tha othar 68K family DMA controllers, the IVR has two addresses (see table 1). Il program compatibility is raquired, the value wntten at tha normal IVR address should have a zero as its LSB, and the value written at the error IVR addrass should be the same but with the LSB equal to one.

DPERATIDN

A DMAI operation proceeds in three principal phases. During the initialization phase, the MPU configures the channel control registers, loads the initial memory address and transfer count, and starts tha channel. During the transfer phasa, the DMAI accepts requests for transfars lrom the device, arbitratas lor and acquires ownership of the bus, and provides loi addressing and bus controls for the transfers. The termination phase occurs after the operation is complete, when the DMAI reports the status of the operation.

Operation Initiation

After having programmed the control registers, the memory address counter, and the memory transfer counter, the MPU sets tha start bit (CCR[7]). The DMAI initiates the operation by clearing any pending requests, clearing the start bit, and setting the channel activa bit in the CSR. The DMAI is then ready to receive valid requasts for an operation.

The channel cannot be started if any of the internal status bits in the CSR (CSR[15:11]) hava not been claarad. An error is not signaled if this condition occurs. The only indication ol this state is that tha start bit ramains set in the CCR. A pending start cannot be resat by a write to the register. START can be cleared only by the DMAI when it starts operation or by setting the software abort bit (CCR[4]).

Device/DMAI Communication

Communication between the periphaial device and the DMAI is accommodated by five signal lines:

Request (REQN)
The device makes a request for service by asserting the request line. The DMAI can operate in either the burst raquast moda or the cycle stealing raquest mode, as programmed by the external request mode bit (DCR[15]).

The burst mode allows a device to request the transfer of multiple operands using consecutive bus cycles. In this mode the request line is an active low input. The DMAI services the requast by arbitrating lor the bus, obtaining the bus, and notifying the peripheral by asserting the acknowledge (ACKN) output. If the request line is active when the DMAI asserts ACKN, and remains active at least until tha DMAI asserts device transfer complete (DTCN), tha DMAI recognizes a valid requast for another operand, which will be transferred during the next bus cycla. If the request line is negated before the DMAI asserts DTCN, the DMAI relinquishes the bus and waits lor the next request. For long word transfars (2 x 16), the request must be asserted at least until the acknowledga for the second part of the operand has been asserted.

In the cycle steal mode, the device requests an operand translar by generating a falling edge on the request line. The DMAI services tha request by arbitrating for the bus, obtaining the bus, and notifying the peripheral by asserting the acknowledge (ACKN) output. The request line must be in the inactive state lor at least one clock cycle before a request is made. After a request has been asserted, it must remain at the assertion level for at least one clock cycle. Il another request is received before the first operand part of a former request is acknowledged, the second request is not recognized. Normally, the DMAI will ralinquish the bus after servicing a valid request. However, il the device generates a new request before the DMAI asserts DTCN lor the last operand part, the DMAI will retain ownership of the bus and that raquest will be serviced before the bus is relinquished.

Acknowledge (ACKN)
The DMAI asserts the acknowledge lina, which implicitly addresses the device making the request, during translers to and from the device. The line may be used to control buffering circuits between the data bus and the MPU bus.

During burst mode, REQN must not be disasserted lor less than one CLK period plus four RC time constants, where R is the value of the rasistor used for tha pullup on BRN and C has a typical value of 20pF.

Ready (RDYN)
Ready is an active low input which is assertad by the requesting devica to indicata to the DMAI that valid data has either been storad or put on the bus. If negated, it indicates that the data has not been stored or presented, causing the DMAI to enter wait states until RDYN is assartad. RDYN can be hald low continuously if the davice is fast enough so that wait states are not required. The currant state ol the ready input is reflected in CSR[8].

Done (DONEN)
Done is a bidirectional active low signal. As an output, it is asserted and negated by the DMAI concurrent with the ACKN output of the last operand part to indicate to the device that the mamory transfar count is exhaustad and that the DMAI's operation is completed as a result of that transfer.

The DMAI also monitors the stata of tha lina while acknowledging a device. If the devica asserts DONEN, the DMAI will terminate operation after the transfer of the current operand. In this case the DMAI clears the channel active bit and sets the channel operation complete and normal devica tarmination bits in the CSR. If both the DMAI and the devica assert DONEN, tha device termination is not recognized, but the operation does terminate.

Device Transfer Complete (DTCN)
DTCN is an active low output which is asserted by the DMAI to indicate to the device that the requastad data transfer is complete. On a write to memory operation, it indicates that the data provided by the device has been successfully stored. On a read from mamory operation, it indicates to the davica that tha data from memory is present on the data bus and should be latched. DTCN is not asserted if assartion of the RERUNN input terminates the bus cycle.

Bus Arbitration

Upon recaiving a valid request for a transfer from the device, tha DMAI will arbitrate for and obtain ownership of the system bus.

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The DMAI indicates that it wishes to become the bus master by asserting its bus request (BRN) output. This is a wire-ORed signal that indicates to the MPU that some external device requires control of the bus. The processor is effectively at a lower priority level than external devices and will relinquish the bus after it has completed the last bus cycle it has started. The processor puts the bus up for external arbitration by asserting its bus grant (BGN) output. This signal may be routed through a daisy chain (such as provided by the DMAI) or through some other priority-encoded network. When the DMAI making the bus request receives the bus grant (indicated by its BGN input being asserted), it is to be the next bus master. It waits until address strobe (ASN), data transfer acknowledge (DTACKN) and bus grant acknowledge (BGACKN) become inactive and then assumes ownership of the bus by asserting its own BGACKN output. The DMAI then negates the BRN output and proceeds with the date transfer phase. After this phase is completed, the DMAI relinquishes bus ownership by negating the BGACKN output.

In burst DMA mode, detection of an active low request input after the DMAI operation has been started will begin the bus arbitration cycle. However, if the device negates its request at least one clock cycle before the DMAI asserts BGACKN, the DMAI will negate its bus request and will not assume ownership of the bus.

Data Transfers

The actual transfer of data between the memory and the device occurs during the data transfer phase. All transfers occur during a single cycle except in the case of long word operands, in which case two cycles are used to transfer the operand as two 16-bit words. The transfers take place using a 'single address' protocol; the DMAI addresses the memory via the bus address lines, while the device is implicitly addressed via the acknowledge output.

When a request is generated using the request method programmed in the control register, the DMAI obtains the bus and asserts acknowledge to notify the device that a transfer is to take place. The DMAI asserts all S68000 bus control signals needed for the transfer and holds them until the device responds with ready. The bus cycle then terminates normally. Ready may be tied low (asserted) if the device is fast enough.

When the transfer is from memory to the device, data is valid when DTACKN is asserted by the memory and remains valid until the data strobe(s) are negated. The assertion of DTCN from the DMAI can be used to latch the data, as the data strobes are not removed until one-half clock after the assertion of DTCN.

When the transfer is from device to memory, the data must be valid on the bus before the DMAI asserts the data strobe(s). The device indicates valid data by asserting ready. The DMAI then asserts the strobes and holds them asserted until the memory accepts the data, indicated by the assertion of DTACKN. The DMAI then asserts DTCN and negates the data strobes.

Flow charts for these operations are shown in figures 1 and 2. Refer to the timing section for the equivalent timing diagrams.

Operation Termination

Termination of the block transfer occurs under the conditions detailed below.

Terminal Count

As part of each transfer of an operand, the DMAI decrements the memory transfer counter. If this counter is decremented to zero, the operand is the last operand of the block. The DMAI operation is complete and it notifies the device of completion by asserting the DONEN output during the last operand transfer cycle. When the transfer has been completed, the channel active bit in the CSR is cleared and the COC bit is set, unless an error occurs.

Device Termination

The DMAI monitors the state of the DONEN line while acknowledging a device transfer request. If the device asserts DONEN, the DMAI will terminate operation after the transfer of the current operand. When the transfer has been completed, the DMAI clears the channel active bit and sets the COC and normal device termination bits in the CSR. If both the DMAI and the device assert DONEN, the device termination is not recognized, but the operation does terminate.

Software Abort

The software abort bit (CCR[4]) allows the MPU to abort the current operation of the DMAI. The COC and error bits in the CSR are set, the channel active bit in the CSR is cleared, and an abort error condition is signaled in the CER.

Rerun Error

The DMAI provides a rerun input (RERUNN) to indicate a bus exception condition. RERUNN must arrive prior to or in coincidence with DTACKN in order to be recognized, and the DMAI verifies that the line has been stable for two clock cycles before acting on it. The occurrence of a rerun during a DMAI bus cycle forces it to terminate the bus cycle in an orderly manner.

When the assertion of rerun is verified, the DMAI stops operation and three-states the data, address, and control lines, except BGACKN, so that it retains ownership of the bus. It remains halted until rerun becomes inactive, and then re-tries the last bus cycle. If rerun is asserted again, the DMAI stops DMA operation, releases the bus, sets the error and COC bits in the CSR, clears the active bit in the CSR, and sets the error code in the CER to indicate a bus error.

While stopped due to assertion of rerun, the DMAI does not generate any bus cycles and will not honor any requests until it is removed. However, the DMAI still recognizes requests.

Error Recovery Procedure

If an error occurs during a DMA transfer such that the DMAI stops the DMA operation, information is available to the operating system for an error recovery routine.

The information available to the operating system consists of the memory address counter, the memory transfer counter, and the control, status, and error registers. The DMAI decrements the memory transfer counter before attempting a DMA operation, so the register will contain the count minus one of the attempted transfer. The memory address counter will contain the address at which the DMA operation was attempted.

Reset

The reset input (RESETN) provides a means of resetting and initializing the DMAI from an external source. If the DMAI is a bus master when reset is received, the DMAI relinquishes the bus. Reset clears the control and error registers, sets all bits of the status register except CSR[6] to zero, and initializes the interrupt vector register to H'0F.

Interrupts

The interrupt enable bit (CCR[3]) determines whether the DMAI generates interrupt requests. When the bit is set, an interrupt request is generated if the channel operation complete bit in the CSR is set. When the IACKN input is asserted, and the DMAI has an interrupt request pending, the DMAI returns an interrupt vector on the data bus.

The interrupt vector issued is the contents of the IVR. Only the seven most significant bits of the programmed value are used by the DMAI. The vector from the DMAI contains a zero in the LSB position if a normal termination occurred (error bit not set) and contains a one in the LSB position if termination was due to an error (error bit set).

The contents of this register are initialized to H'0F' by a reset. The value returned will be H'0F', regardless of the error state, until the register is programmed by the MPU.

To provide compatibility with the other 68K family DMA controllers, the IVR has two addresses (see table 1). If program compatibility is required, the value written at the

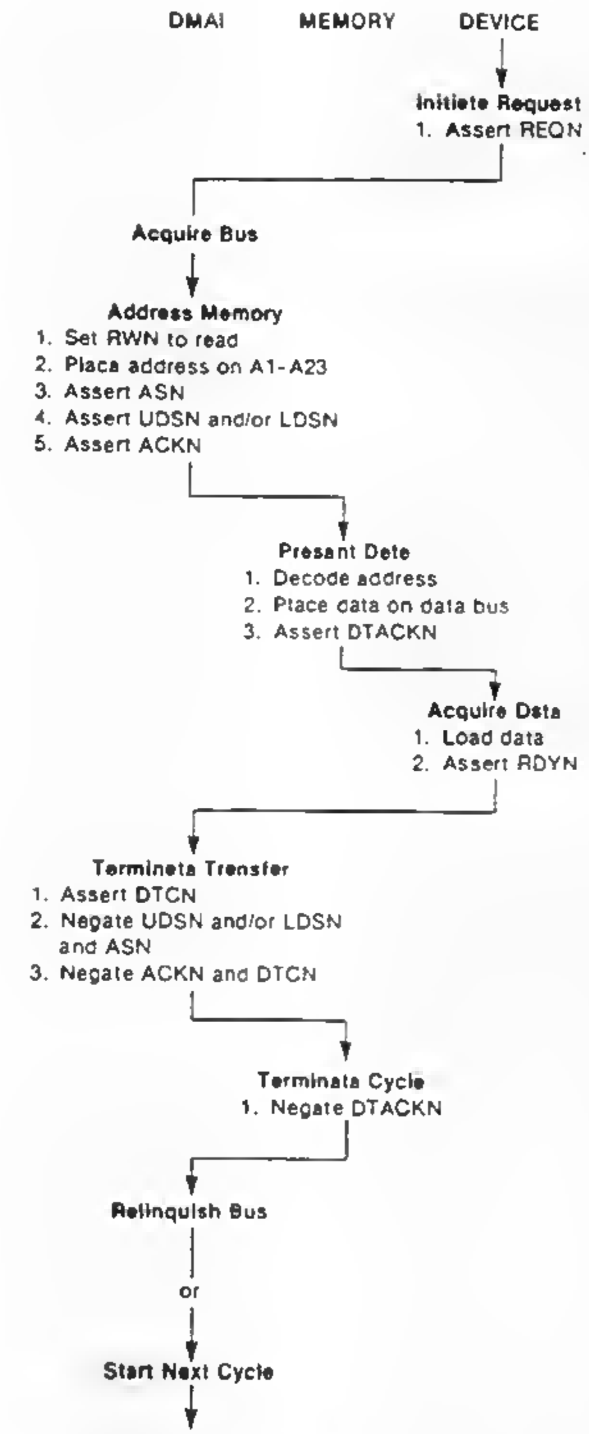

Figure 1. Transfer from Memory to Device Flowchart

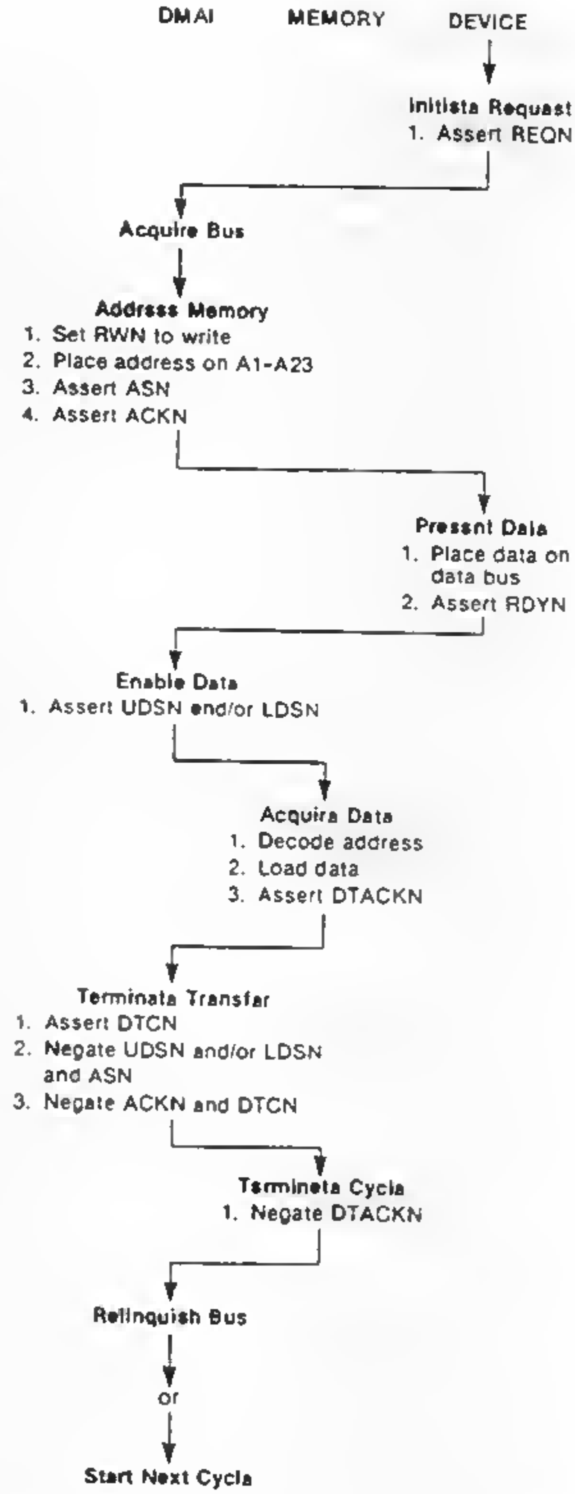

Figure 2. Transfer from Device to Memory Flowchart

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normal IVR address should have a zero as its LSB, and the value written at the error IVR address should be the same but with the LSB equal to one.

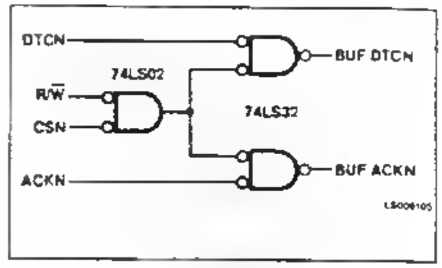
APPLICATIONS

Figure 3 illustrates a typical interconnection of the DMAI in a 68000 based system.

DESIGN NOTE

When clearing the error bit in CSR (bit 12) after a DMAI abort due to a double RERUNN, ACKN and DTCN will both go low concurrent with CSN and DTACKN for one CLK cycle.

To prevent the possibility that the device may misinterpret these signals, it is suggested that these signals be ANDed with CSN (see figure below).



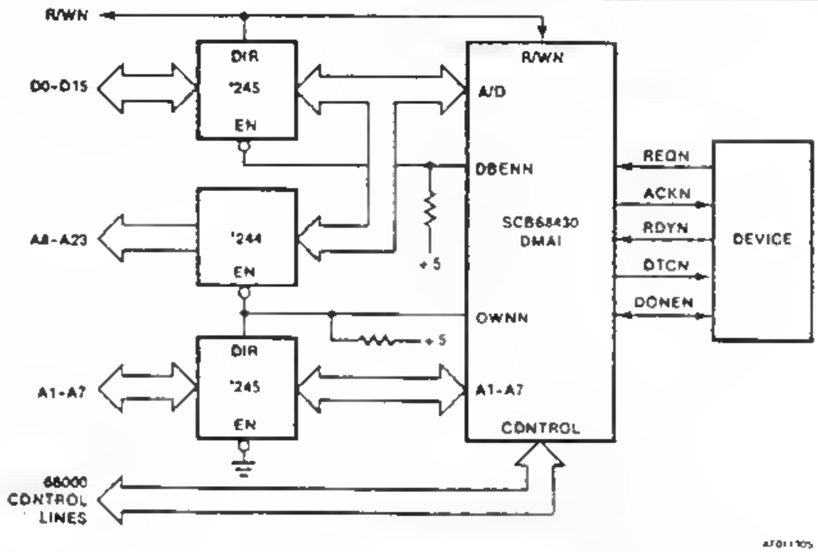


Figure 3. DMAI Application

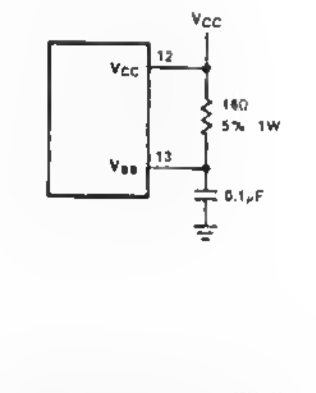


Figure 4. Recommended V_{BB} Test Circuit

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Supply voltages V_{CC} and V_{BB}	−0.5 to +7.0	V
Input voltage	−0.5 to +5.5	V
Operating temperature range[2]	0 to +70	°C
Storage temperature	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±5%, V_{BB} = Figure 4, T_A = 0°C to +70°C[3,4,7]

	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Max	UNIT
V_{IL}	Input low voltage			0.8	V
V_{IH}	Input high voltage		2.0		V
V_{OL}	Output low voltage	I_{OUT} = 5.3mA		0.5	V
V_{OH}	Output high voltage, all outputs except open collector outputs[5]	I_{OUT} = −400μA	2.5		V
I_{IL}	Input low current	V_{IN} = 0.4V		−400	μA
I_{IH}	Input high current	V_{IN} = 2.7V		20	μA
I_{OC}	Open collector off state current[5]	V_{OUT} = 2.4V		20	μA
I_{SC}	Output short circuit current[6]	V_{CC} = max	−40	−100	mA
I_{CC}	V_{CC} supply current	V_{CC} = max		130	mA
I_{BB}	V_{BB} supply current	V_{CC} = max		275	mA

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or at any other conditions other than those indicated in the Electrical Characteristics section of this data sheet is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. Parameters are valid over specified temperature range.
4. All voltage measurements are referenced to ground (V_{SS}). For testing, all signals swing between 0.4V and 2.4V with a transition time of 20ns maximum. All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate.
5. IRQN, BRN, DONEN, and OWNN are open collector outputs.
6. No more than one output should be connected to ground at one time.
7. Capacitive test load is 100pF for all pins except DTCN which has a 35pF capacitive test load.

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±5%, V_{BB} = Figure 4, T_A = 0°C to +70°C[3,4,7]

NO.	FIGURE	CHARACTERISTICS	TENTATIVE LIMITS 10MHz Min	10MHz Max	12.5MHz Min	12.5MHz Max	UNIT
1	5	A1−A7, ASN, RWN, set-up to UDSN, LDSN low	0		0		ns
2	5	D0−D15 3-state to invalid data from ASN, CSN, and UDSN or LDSN low	10		10		ns
3	5	DTACKN 3-state to high from ASN, CSN, and UDSN or LDSN low	10		10		ns
4	5	CSN low after UDSN or LDSN low		25		25	ns
5	5, 6	DBENN low after ASN and CSN low		60		60	ns
6	5	D0−D15 valid data from ASN, CSN, and UDSN or LDSN low		100		100	ns
7	5	DTACKN low after D0−D15 valid data	−15	30	−15	30	ns
8	5	A1−A7, ASN, RWN or CSN hold after UDSN and LDSN high	0		0		ns
9	5, 6	DBENN high from either ASN or CSN high		45		45	ns
10	5	D0−D15 to 3-state from UDSN and LDSN high		80		80	ns
11	5	D0−D15 to invalid data from UDSN and LDSN high	10		10		ns
12	5, 6	DTACKN high from UDSN and LDSN high		55		55	ns
13	5, 6	DTACK 3-state from either CSN or ASN high		85		85	ns
14	6	A1−A7, ASN, RWN set-up to UDSN, LDSN low	50		50		ns/s
15	6	CSN set-up before UDSN or LDSN low	20		20		ns
16	6	DTACKN 3-state to high after CSN and ASN low	10		10		ns
17	6	D0−D15 valid after UDSN or LDSN low		0		0	ns
18	6	DTACKN low from UDSN or LDSN low		100		100	ns
19	6	UDSN and LDSN low time	115		100		ns
20	6	A1−A7 hold after UDSN and LDSN high	0		0		ns
21	6	ASN, RWN and CSN hold after UDSN and LDSN high	0		0		ns

AC ELECTRICAL CHARACTERISTICS (Continued)

NO.	FIGURE	CHARACTERISTICS	TENTATIVE LIMITS				UNIT
			10MHz		12.5MHz		
			Min	Max	Min	Max	
22	6	D0 – D15 hold after UDSN and LDSN high	0		0		ns
23	7	DBENN low from last low of ASN, IACKN, LDSN		65		65	ns
24	7	D0 – D7 valid after last low of ASN, IACKN, LDSN		105		105	ns
25	7	DTACKN 3-state to high after last low of ASN, IACKN, LDSN		100		100	ns
26	7	DTACKN low after last low of ASN, IACKN, LDSN		110		110	ns
27	7	DBENN high after first high of ASN, IACKN, LDSN		55		55	ns
28	7	D0 – D7 hold after first high of ASN, IACKN, LDSN		60		60	ns
29	7	D0 – D7 3-state after first high of ASN, IACKN, LDSN		80		80	ns
30	7	DTACKN high after first high of ASN, IACKN, LDSN		60		60	ns
31	7	DTACKN 3-state after first high of ASN, IACKN, LDSN		95		95	ns
32	8	BRN high from CLK high		65		65	ns
33	8, 11, 12	BGACKN low from CLK low		75		75	ns
34	8, 11, 12	OWNN low from CLK high		75		75	ns
35	8	BGACKN high from CLK low		75		75	ns
36	8,11,12	OWNN high from CLK high (load dependent)		50		50	ns
37	10	REQN set-up before CLK low	30		30		ns
38	10	REQN hold after CLK high	20		20		ns
39	10	BRN low from CLK high		80		80	ns
41	11, 12	ASN, UDSN, LDSN, RWN 3-state to high from CLK low		75		75	ns
43	11, 12	A1 – A23 to valid ASN	0		0		ns
44	11, 12	ASN low from CLK high		65		65	ns
45	11, 12	LDSN, UDSN low from CLK high		90		90	ns
46	11, 12	ACKN low from CLK high		65		65	ns
47	11, 12	DTACKN set-up to CLK high	30		30		ns
48	11, 12	RDYN set-up to CLK low	30		30		ns
49	11, 12	DTCN low from CLK high		70		70	ns
50	11, 12	ASN high from CLK high		75		75	ns
51	11, 12	LDSN, UDSN, high from CLK high		90		90	ns
52	11, 12	DTACKN, RDYN hold after CLK high	0		0		ns
–	11, 12	ASN, LDSN, UDSN, high from DTCN low	-20		-20		ns
53	11, 12	ACKN high from CLK high		50		50	ns
54	11, 12	DTCN high from CLK high		50		50	ns
55	11, 12	Address valid after CLK low	10		10		ns
–	11, 12	Address valid after ASN high	0		10		ns
56	11, 12	DONEN (output) low from CLK low		120		120	ns
57	11, 12	DONEN (output) high from CLK high		50		50	ns
58	11, 12	DONEN (input) set-up low before CLK low	30		30		ns
59	11, 12	DONEN (input) hold low after CLK high	0		0		ns
60	11, 12	BGACKN, ASN, UDSN, LDSN, RWN to 3-state from CLK low		75		75	ns
62	11, 12	A1 – A23 valid to 3-state from CLK high		100		100	ns
63	12	R/WN low from CLK high		65		65	ns
64	12	R/WN high from CLK high		75		75	ns
65	13	RERUNN set-up low before CLK high	30		30		ns
66	13	RERUNN hold low from CLK high	20		20		ns
67	13	A1 – A23 to idle state from CLK low		100		100	ns
68	13	A1 – A23 to valid after CLK low		85		85	ns

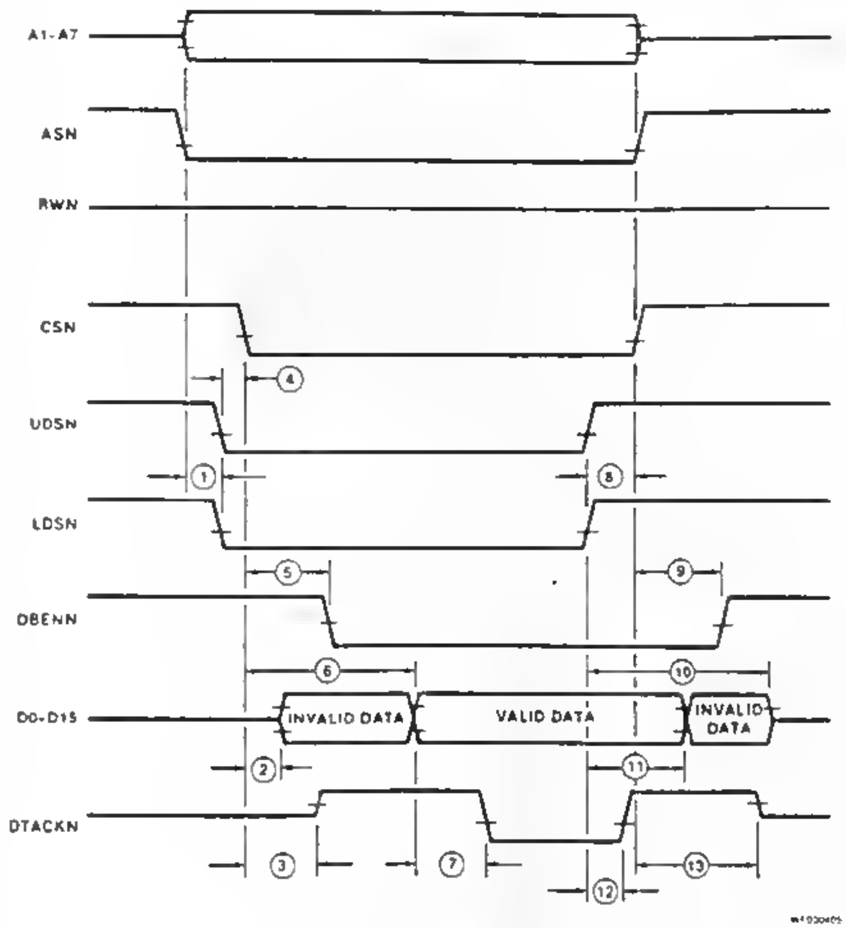


Figure 5. DMAI Read Timing

Direct Memory Access Interface (DMAI) SCB68430

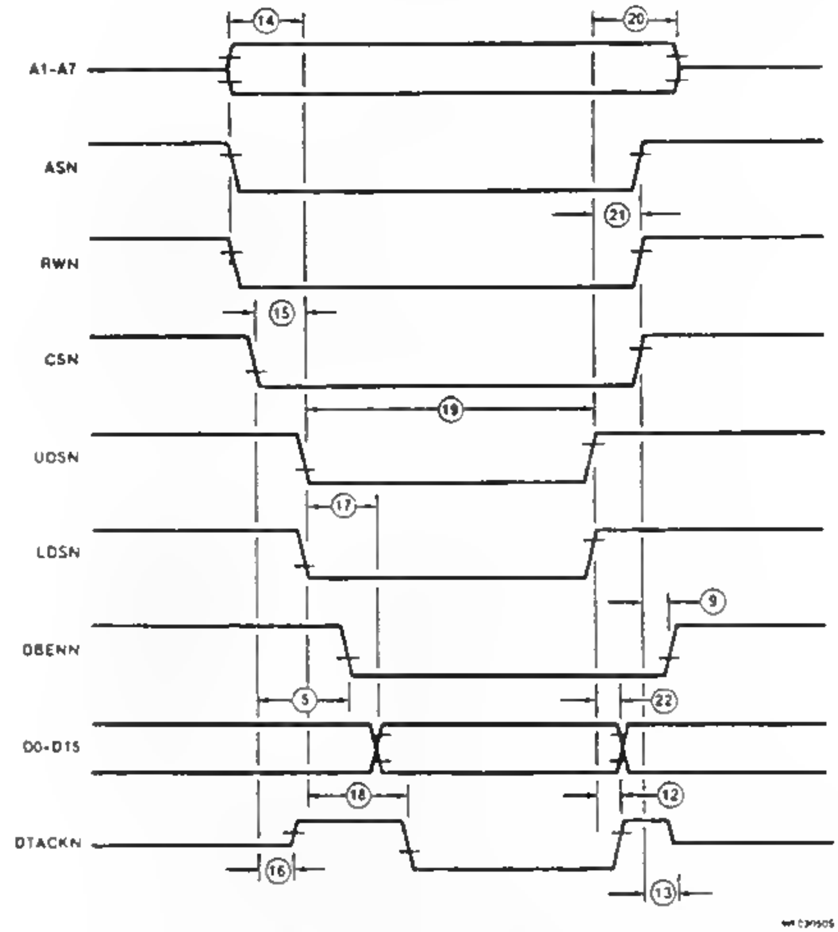


Figure 6. DMAi Write Timing

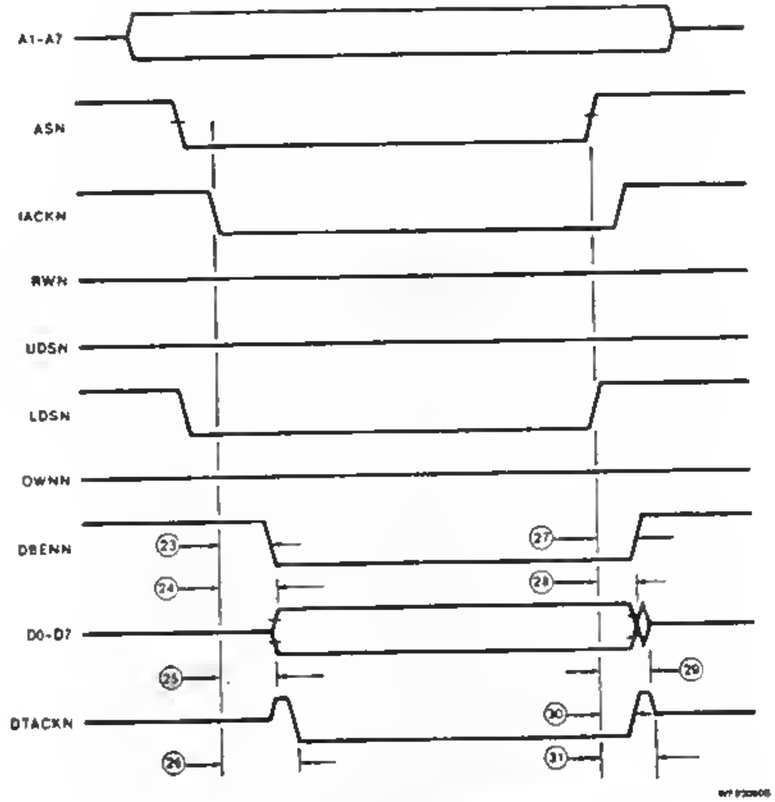
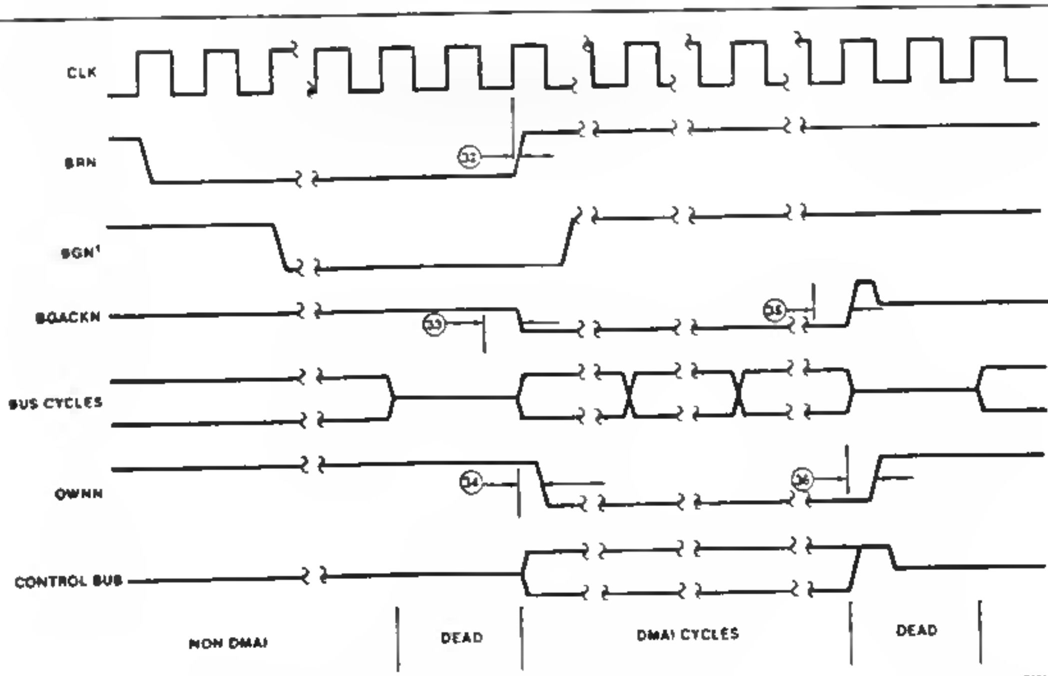
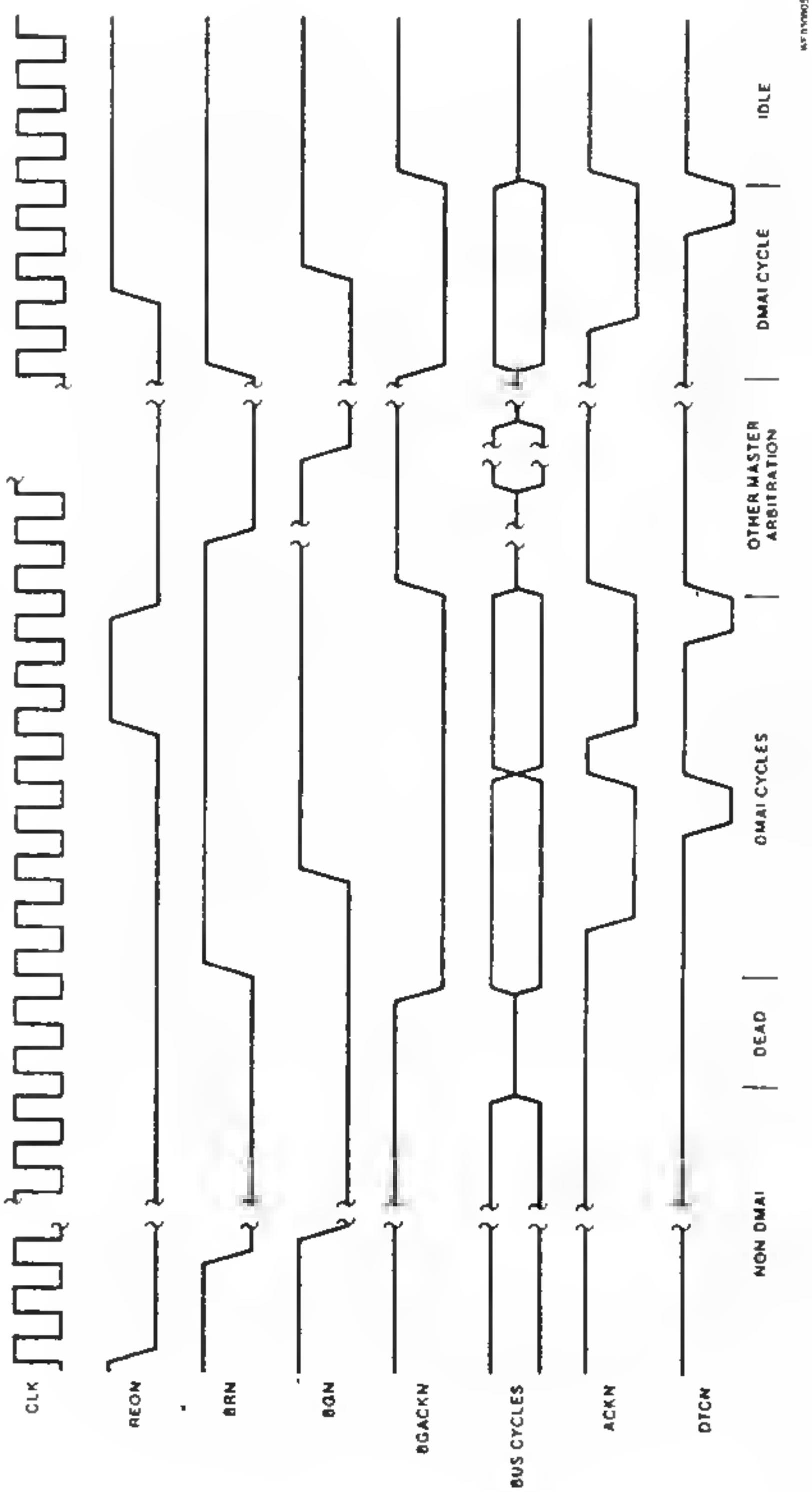


Figure 7. CPU IACK Cycle to DMAI



NOTES:
1. Device will become master if BGN is asserted concurrent with or later than REQN (same clock edge or later).
2. ASN, DTACKN and BGACKN must be negated in order for DMAI to become master. Timing assumes all these happen concurrent with BGN — if not, it is from the latest signal which is negated.

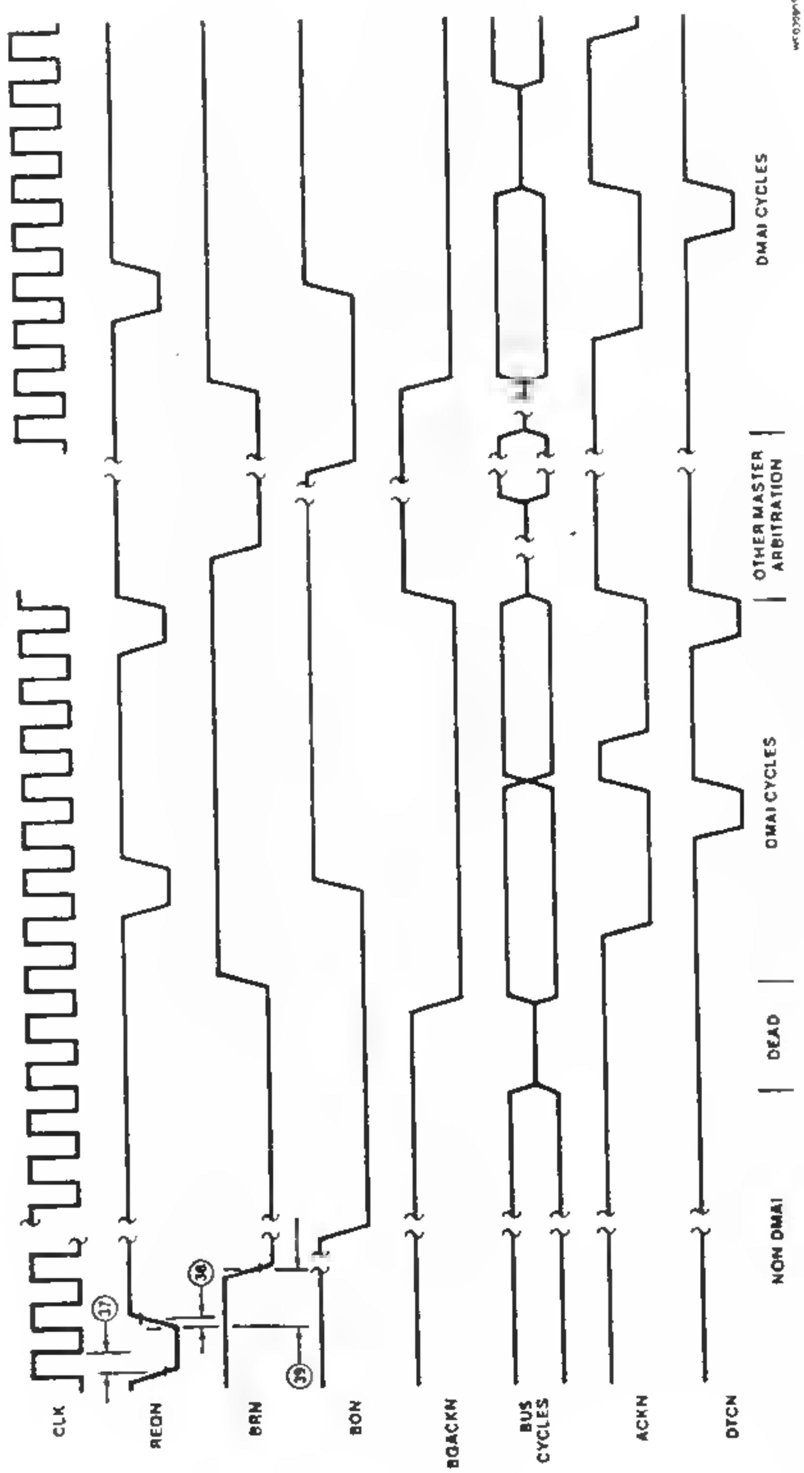
Figure 8. DMAI Bus Arbitration Timing



NOTES:
1. To maintain mastership next bus cycle, REQN must remain asserted at least until 1/2 clock cycle after DTCN is asserted.
2. To guarantee that mastership is relinquished next cycle, REQN must be negated no later than 1/2 clock cycle prior to DTCN

Figure 9. DMAI Burst Mode Request Timing

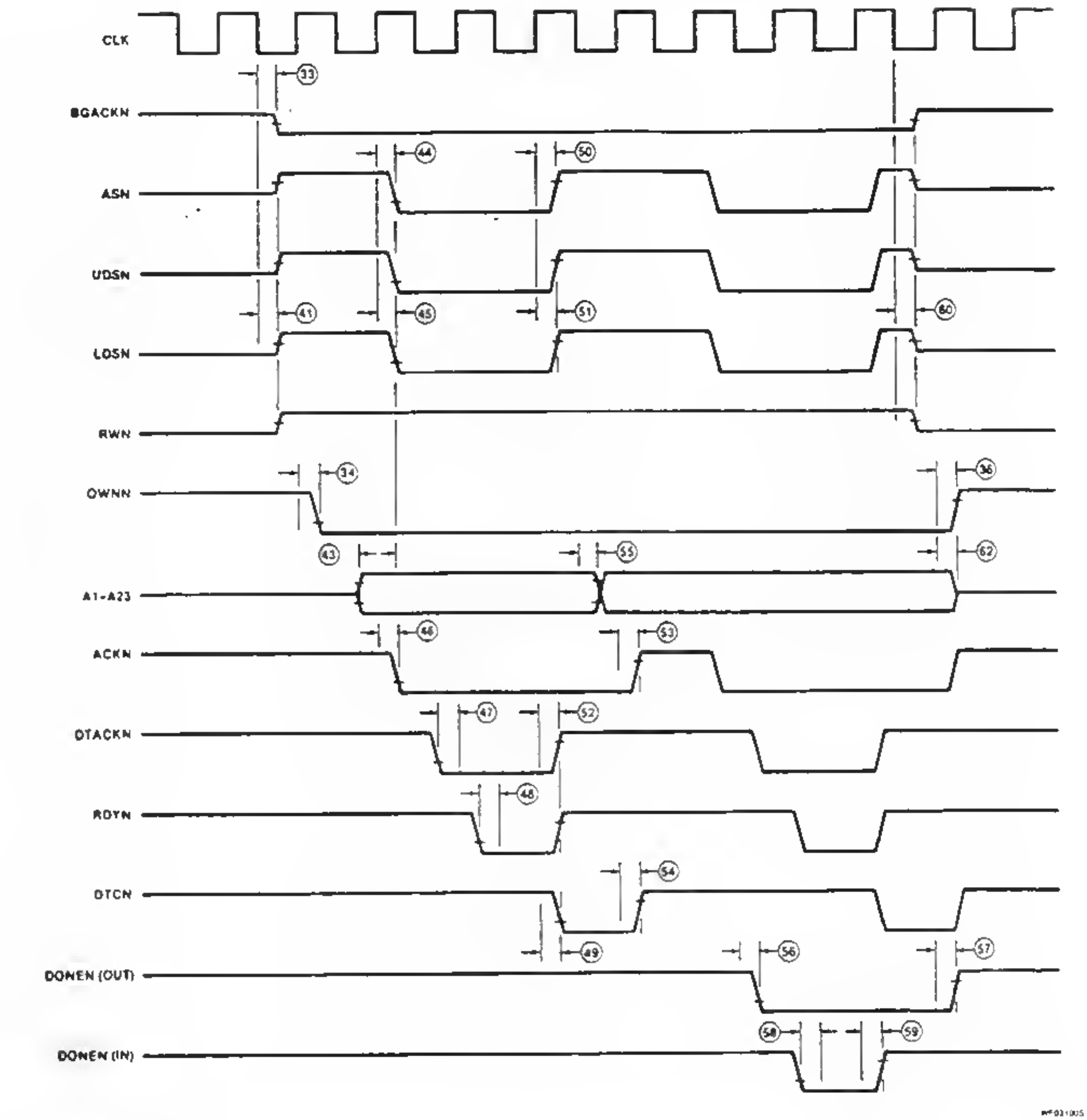
Direct Memory Access Interface (DMAI) SCB68430



1. In order to keep the bus, REQN must come no later than the 1/2 clock minus the set-up time 57 prior to assertion edge of DTCN

Figure 10. DMAI Cycle Steal Mode Request Timing

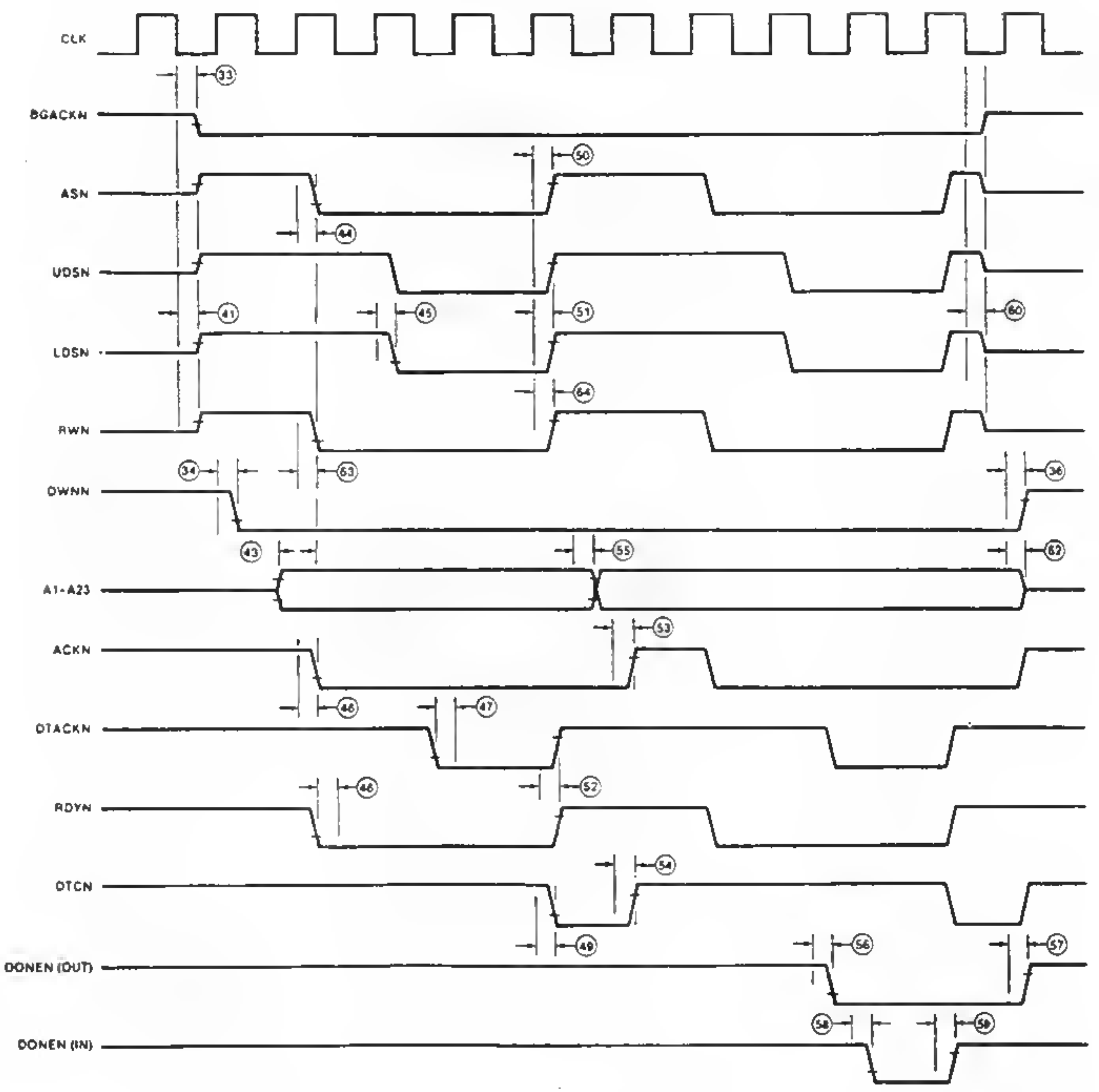
Direct Memory Access Interface (DMAI) SCB68430



NOTE:
1. 16-bit transfer illustrated. For 8-bit transfer either LDSN or UDSN, but not both, will be asserted each cycle, depending on byte address.

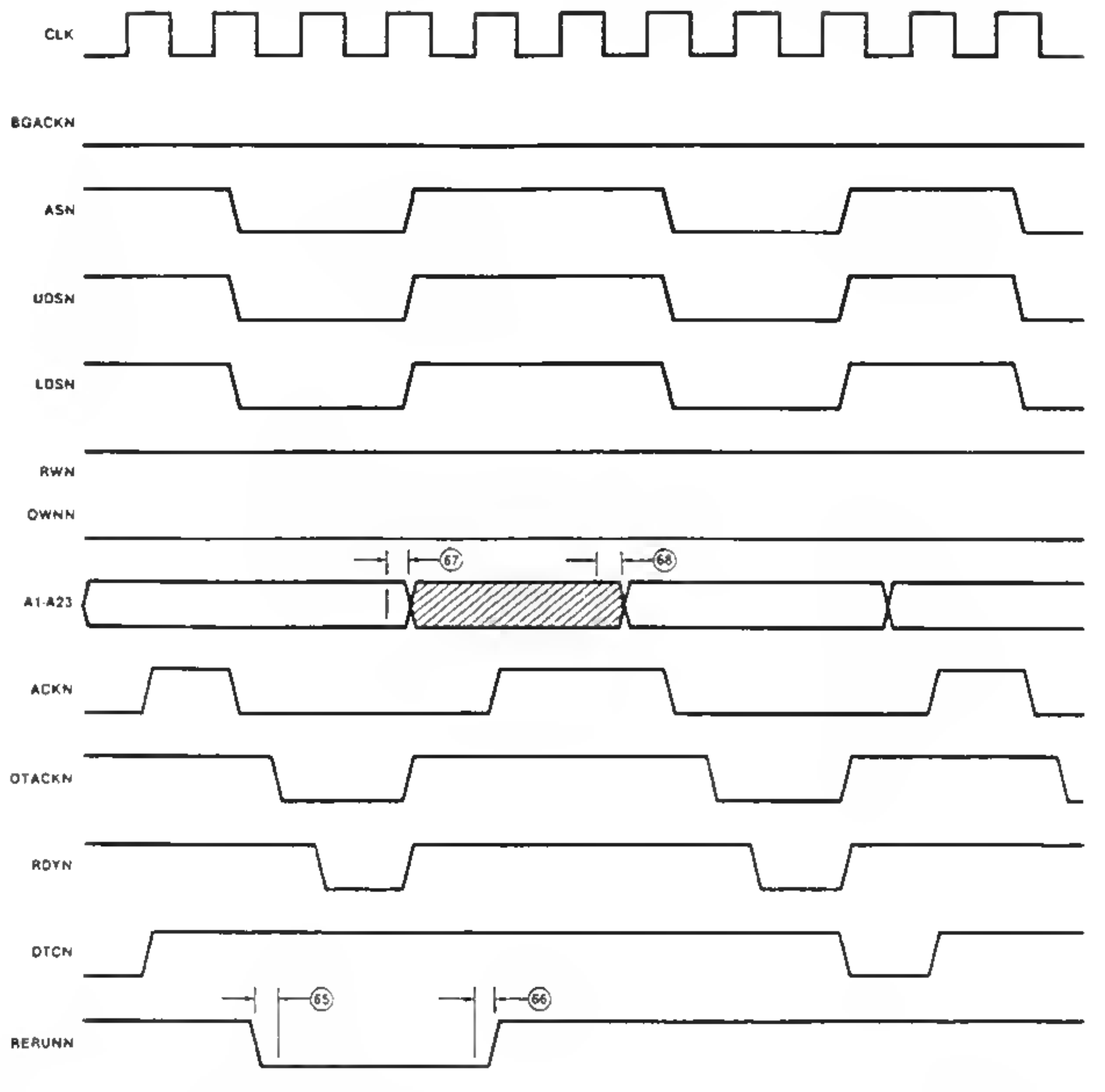
Figure 11. Read from Memory, Write to Device

Direct Memory Access Interface (DMAI) SCB68430



NOTE:
1. 16-bit transfer illustrated. For 8-bit transfer either LDSN or UDSN, but not both, will be asserted each cycle, depending on byte address.

Figure 12. Write to Memory, Read from Device



NOTES:
1. 16-bit transfer illustrated. For 8-bit transfer either LDSN or UDSN, but not both, will be asserted each cycle, depending on byte address
2. DMAI will release the bus after a RERUNN if there is no valid request. The next request will then retry the cycle which was terminated by the RERUNN signal
3. RERUNN must be asserted no later then DTACKN and RDYN
4. If a cycle is terminated by RERUNN, the transfer count will be one less than the actual data transferred correctly. The double RERUNN signal on the same cycle will terminate the DMAI operation with a status bit set and an interrupt generated (if enabled)

Figure 13. Rerun Asserted During Read from Memory, Write to Device

APPENDIX C

DMA Test Software Listing

The following two software listings, DMABTM and DMABTS, are included as examples for test software that can be utilized for testing the VMIVME-DMA Boards in a back-to-back mode.

```
                            ************************************************************************
                            ******              THIS PART OF THE TEST SOFTWARE IS                 ******
                            ******                 FOR THE MASTER'S CHASSIS                       ******
                            ************************************************************************
                            ******   THIS DMA TEST TESTS 2 DMA'S IN BACK TO BACK MODE              ******
                            ******   IN SEPERATE CHASSIS. THE TEST PREFORMS DMA TRANSFERS IN       ******
                            ******   BOTH DIRECTIONS IN CYCLE STEAL AND BURST MODES.  SET JUMPERS  ******
                            ******   AS SHOWN IN THE MANUAL FOR BUS REQUEST LEVEL 3 AND GRANT LEVEL ******
                            ******   3.  CABLE P3 TO P3 AND P4 TO P4.  BOARD BASE                  ******
                            ******   ADDRESS IS SET FOR $E000. RUN THIS SOFTWARE IN CHASSÍS ONE.   ******
                            ******   CREATED APRIL 23, 1988 BY MGL. REV1                           ******
                            ******   REV2 JAN 11, 1988 CONTINOUS LOOP ADDED BY MGL                 ******
                            ************************************************************************

          00001000                  ORG.S    $1000
 00001000 3E7C1F00                  MOVE.W   #$1F00,A7           INITIALIZE STACK POINTER
 00001004 4DFB125A                  LEA      MSG8,A5             SIGNON MESSAGE
 00001008 4DFB129E                  LEA      EHMSG8,A6
 0000100C 4E4F                      TRAP     #15
 0000100E 0006                      DC.W     6

 00001010 123C00B8        START     MOVE.B   #$B8,D1             SETUP D1 FOR TRANSFER IN CYCLE STEAL
 00001014 4246                      CLR      D6

 00001016 283C5A5A5A5A START1       MOVE.L   #$5A5A5A5A,D4       FIRST DATA PATTERN TO BE TRANSFERED
 0000101C 612A                      BSR.S    LDMEM1
 0000101E 613A                      BSR.S    DMAOUT

 00001020 283CA5A5A5A5              MOVE.L   #$A5A5A5A5,D4       SECOND DATA PATTERN
 00001026 6120                      BSR.S    LDMEM1
 00001028 6130                      BSR.S    DMAOUT

 0000102A 7800                      MOVE.L   #$00000000,D4       THIRD  DATA PATTERN
 0000102C 611A                      BSR.S    LDMEM1
 0000102E 612A                      BSR.S    DMAOUT

 00001030 78FF                      MOVE.L   #$FFFFFFFF,D4       FORTH DATA PATTERN
 00001032 6114                      BSR.S    LDMEM1
 00001034 6124                      BSR.S    DMAOUT
 00001036 0C060008                  CMP.B    #8,D6
 0000103A 6708                      BEQ.S    DIN
 0000103C 123C0028                  MOVE.B   #$28,D1             SET TRANSFER FOR BURST MODE
 00001040 4EF01016                  JMP.S    START1
 00001044 4EF010FB        DIN       JMP.S    START3

 00001048 41F900040000 LDMEM1       LEA      $40000,A0           LOAD MEM. WITH DATA PATTERN
 0000104E 20C4            INITMEM1  MOVE.L   D4,(A0)+
 00001050 B1FC00041000              CMPA.L   #$41000,A0
 00001056 66F6                      BNE      INITMEM1
 00001058 4E75                      RTS

                            ************************************************************************
                            *****TRANSFER DMA BLOCK OUT*********************************************
                            ************************************************************************


 0000105A 46FC2700        DMAOUT    MOVE.W   #$2700,SR           MASK INTERUPTS
 0000105E 163C0000                  MOVE.B   #0,D3
```

```
00001062 13FC004500FF         MOVE.B  #$45,$FFE040        LOAD ATTN. INTERRUPT VECTOR
         E040
0000106A 13FC004000FF         MOVE.B  #$40,$FFE025        LOAD DMA INTERRUPT VECTOR
         E025
00001072 13FC000B00FF         MOVE.B  #$B,$FFE007         ENABLE DMA INTERRUPTS
         E007
0000107A 13C100FFE004         MOVE.B  D1,$FFE004          SET UP TRANSFER TYPE
00001080 13FC00B000FF         MOVE.B  #$B0,$FFE000        CLEAR CSR
         E000
00001088 13FC003900FF         MOVE.B  #$39,$FFE065        LOAD LWORD# AND ADDRESS MODIFIER
         E065
                       ***********************************************************************
                       ***********68000 TYPE CPU'S MULTIPLY THE INTERRUPT VECTOR BY 4*****************
                       ***********DURING AN INTERRUPT CYCLE.  EXAMPLE :  $45 *$4 = $114***************
                       ***********************************************************************

00001090 21FC0000110B         MOVE.L  #ATTN,$114          ATTN INT VECTOR LOCATION
         0114
00001098 21FC000011AE         MOVE.L  #DONE1,$100         DMA DONE VECTOR LOCATION
         0100
000010A0 21FC000011FA         MOVE.L  #I13,$104           DMA ERROR VECTOR TO LOCATION I13
         0104
                       ***********************************************************************



000010A8 33FC040000FF         MOVE.W  #$400,$FFE00A       LOAD TRANSFER COUNT
         E00A
000010B0 23FC00040000         MOVE.L  #$40000,$FFE00C     LOAD MEM ADD COUNTER
         00FFE00C
000010BA 13FC003200FF         MOVE.B  #$32,$FFE005        LOAD OCR
         E005
000010C2 13FC001E00FF         MOVE.B  #$1E,$FFE045        ATTN CONTROL REG. LEVEL 6 INT.
         E045
000010CA 13FC000B00FF         MOVE.B  #$0B,$FFE061        SET SPARE BIT TO DMA2 BOARD
         E061
000010D2 267C00FFE060 WAIT    MOVE.L  #$FFE060,A3
000010D8 3813                 MOVE.W  (A3),D4             WAIT FOR DMA2 TO RESPOND
000010DA 02440080             AND.W   #$0080,D4           WITH SPARE BIT SET
000010DE 0C440080             CMP.W   #$0080,D4
000010E2 66EE                 BNE.S   WAIT
000010E4 13FC001200FF         MOVE.B  #$12,$FFE061        ENABLE ATTN OUT,ATTN IN
         E061
000010EC 46FC2000             MOVE.W  #$2000,SR
000010F0 0C030001     SELF1   CMP.B   #1,D3               WAIT FOR SOMETHING TO HAPPEN
000010F4 66FA                 BNE.S   SELF1
000010F6 4E75                 RTS


                       ***********************************************************************
                       *********RECIEVE DMA BLOCK**********************************************
                       ***********************************************************************

000010F8 123C0000     START3  MOVE.B  #$00,D1             SET TRANSFER TO CYCLE STEAL
000010FC 1C3C0000             MOVE.B  #0,D6
00001100 13FC000000FF         MOVE.B  #0,$FFE063          FAIL LED ON
         E063

00001108 283C5A5A5A5A START2  MOVE.L  #$5A5A5A5A,D4       FIRST DATA PATTERN RECIEVED
0000110E 6122                 BSR.S   DMAIN
```

```

00001110 203CA5A5A5A5         MOVE.L  #$A5A5A5A5,D4        SECOND DATA PATTERN RECIEVED
00001116 611A                 BSR.S   DMAIN

00001118 7000                 MOVE.L  #$00000000,D4        THIRD DATA PATTERN RECIEVED
0000111A 6116                 BSR.S   DMAIN

0000111C 70FF                 MOVE.L  #$FFFFFFFF,D4        FORTH DATA PATTERN RECIEVED
0000111E 6112                 BSR.S   DMAIN
00001120 0C060008             CMP.B   #8,D6                COUNT THE NUMBER OF BLOCKS RECIEVED
00001124 6708                 BEQ.S   DOUT
00001126 123C0020             MOVE.B  #$20,D1              SET TRANSFER TO BURST MODE
0000112A 4EF81108             JMP.S   START2
0000112E 4EF81018     DOUT    JMP.S   START


00001132 46FC2700     DMAIN   MOVE.W  #$2700,SR            MASK INTERRUPTS
00001136 163C0000             MOVE.B  #0,D3
0000113A 33FC0400FF           MOVE.W  #$400,$FFE00A        LOAD TRANSFER COUNT
         E00A
00001142 23FC00041000         MOVE.L  #$41000,$FFE00C      LOAD MEM ADD COUNT
         00FFE00C
0000114C 13FC00B000FF         MOVE.B  #$B0,$FFE000         CLEAR CSR
         E000
00001154 13C100FFE004         MOVE.B  D1,$FFE004           SET TRANSFER TYPE
0000115A 13FC00B200FF         MOVE.B  #$B2,$FFE005         LOAD OCR
         E005
00001162 13FC004400FF         MOVE.B  #$44,$FFE040         LOAD ATTN INT VECTOR
         E040
0000116A 13FC004600FF         MOVE.B  #$46,$FFE025         LOAD DMA INT VECTOR
         E025
00001172 21FC000011BE         MOVE.L  #ATTN1,$110          ATTN VECTOR LOCATION
         0110
0000117A 21FC000011FA         MOVE.L  #I13,$11C            DMA ERROR
         011C
00001182 21FC0000121A         MOVE.L  #DONE2,$118          DMA DONE VECTOR
         0118
0000118A 13FC003900FF         MOVE.B  #$39,$FFE065         LOAD LWORD* ADDR MODIFIER
         E065
00001192 13FC001000FF         MOVE.B  #$10,$FFE045         ATTN CONTROL REG,LEVEL 5 INT.
         E045
0000119A 13FC001000FF         MOVE.B  #$10,$FFE061         ENABLE ATTN. INT
         E061
000011A2 46FC2000             MOVE.W  #$2000,SR
000011A6 0C030001     SELF2   CMP.B   #1,D3                WAIT FOR INTERRUPT
000011AA 66FA                 BNE.S   SELF2
000011AC 4E75                 RTS


                      ***************DONE1 INTERRUPT SERVICE ROUTINE**********************************
000011AE 5206         DONE1   ADD.B   #1,D6
000011B0 163C0001             MOVE.B  #1,D3
000011B4 13FC000000FF         MOVE.B  #$00,$FFE063
         E063
000011BC 4E73                 RTE

                      **************ATTN1 INTERRUPT SERVICE ROUTINE***********************************
000011BE 13FC003D00FF ATTN1   MOVE.B  #$30,$FFE047         ENABLE DMA INT
```

```
                  E047
00011C6 13FC00BB00FF           MOVE.B   #$BB,$FFE007          START DMA CONTROLER
        E007
000011CE 13FC00B300FF          MOVE.B   #$B3,$FFE061          ENABLE ATTN INT OUT, GO BIT SET, RECEIVE
        E061
000011D6 4E73                  RTE

                       ************ATTN INTERRUPT SETVICE ROUTINE*************************************

000011D8 13FC00B000FF ATTN     MOVE.B   #$B0,$FFE063          ATTN SERVICE ROUTINE
        E063
000011E0 13FC003D00FF          MOVE.B   #$3D,$FFE047          LOAD DICR (ENA DMA INTERRUPT)
        E047
000011E8 13FC00BB00FF          MOVE.B   #$BB,$FFE007          START DMA CONTROLER
        E007
000011F0 13FC000500FF          MOVE.B   #$05,$FFE061          HIT GO BIT TO ENABLE HANDSHAKE, CYCLE
        E061
000011F8 4E73                  RTE


000011FA 4BFB1205     113      LEA.L    MSG3,A5               DMA ERROR SERVICE ROUTINE
000011FE 4DFB1219              LEA.L    ENMSG3,A6
00001202 4E4F                  TRAP     #15
00001204 00                    DC.B     0

00001205 0D0A         MSG3     DC.B     $D,$A
00001207 4D4153544552          DC.B     'MASTER DMA ERROR'
00001217 0D0A                  DC.B     $D,$A
00001219              ENMSG3

                       ****************************************************************************
                       ******DONE2 INTERRUPT SERVICE ROUTINE ****************************************
                       ****************************************************************************
                       ***THIS SERVICE ROUTINE CHECKS THE RECIEVER BUFFER FOR DATA ERRORS************
                       ****************************************************************************

0000121A 5206         DONE2    ADD.B    #1,D6
0000121C 163C0001              MOVE.B   #1,D3
00001220 287C00041000          MOVE.L   #$41000,A4            STARTING ADDRESS OF RECIEVER BUFFER
00001226 303C0000              MOVE.W   #0,D0
0000122A 2A1C         NOSHIFT  MOVE.L   (A4)+,D5
0000122C BA84                  CMP.L    D4,D5                 COMPARE BUFFER
0000122E 660A                  BNE.S    DATAERR
00001230 5240                  ADD.W    #1,D0
00001232 0C400400              CMP.W    #$400,D0
00001236 66F2                  BNE.S    NOSHIFT
00001238 4E73                  RTE

0000123A 4BFB124A     DATAERR  LEA      DERR,A5
0000123E 4DFB125A              LEA      ENDERR,A6
00001242 4E4F                  TRAP     #15
00001244 0006                  DC.W     6
00001246 4E4F                  TRAP     #15
00001248 0000                  DC.W     0

0000124A 0D0A         DERR     DC.B     $D,$A                 SCREEN PRINTED MESSAGES
0000124C 444154412045          DC.B     'DATA ERROR'
00001256 0D0A                  DC.B     $D,$A
```

```
00001258 0D0A                   DC.B     $D,$A
0000125A              ENDERR

0000125A 0D0A         MS68      DC.B     $D,$A
0000125C 445231315720           DC.B     'DR11W TEST IS IN PROGRESS'
00001275 0D0A                   DC.B     $D,$A
00001277 464C41534849           DC.B     'FLASHING LEDS INDICATE A PASSING TEST'
0000129C 0D0A                   DC.B     $D,$A
0000129E              ENMS68
                                END

****** TOTAL ERRORS      0--
****** TOTAL WARNINGS    0--
```

SYMBOL TABLE LISTING

SYMBOL NAME	SECT	VALUE	SYMBOL NAME	SECT	VALUE
ATTN		000011D8	I13		000011FA
ATTN1		000011BE	INITMEM1		0000104E
DATAERR		0000123A	LDMEM1		00001048
DERR		0000124A	MSG3		00001205
DIN		00001044	MSG8		0000125A
DMAIN		00001132	NOSHIFT		0000122A
DMAOUT		0000105A	SELF1		000010F0
DONE1		000011AE	SELF2		000011A6
DONE2		0000121A	START		00001010
DOUT		0000112E	START1		00001016
ENDERR		0000125A	START2		000011B8
ENMSG3		00001219	START3		000010FB
ENMSG8		0000129E	WAIT		000010D2

```
                              ***************************************************************************
                              *****              THIS PART OF THE TEST SOFTWARE IS                 *****
                              *****                  FOR THE SLAVE'S CHASSIS                       *****
                              ***************************************************************************
                              ******  THIS DMA TEST TESTS 2 DMA'S IN BACK TO BACK MODE             *****
                              ******  IN SEPERATE CHASSIS. THE TEST PREFORMS DMA TRANSFERS IN       *****
                              ******  BOTH DIRECTIONS IN CYCLE STEAL AND BURST MODES.  SET JUMPERS  *****
                              ******  AS SHOWN IN THE MANUAL FOR BUS REQUEST LEVEL 3 AND GRANT LEVEL *****
                              ******  3. CABLE P3 TO P3 AND P4 TO P4.  BOARD BASE                  *****
                              ******  ADDRESS IS SET FOR $E000. RUN THIS SOFTWARE IN CHASSIS TWO.  *****
                              ******  CREATED FEB. 23, 1988 BY MBL. REV1                           *****
                              ***************************************************************************


              00001000                ORG.S    $1000
    00001000 3E7C1F00                 MOVE.W   #$1F00,A7          INITALIZE STACK POINTER
    00001004 4BF8126C                 LEA      MSGB,A5
    00001008 4DF812AE                 LEA      ENMSGB,A6          SIGN ON MESSAGE
    0000100C 4E4F                     TRAP     #15
    0000100E 0006                     DC.W     6

    00001010 4245            RESTART  CLR      D5
    00001012 13FC000000FF             MOVE.B   #$00,$FFE063
             E063
    0000101A 1C3C0000                 MOVE.B   #0,D6
    0000101E 123C0088                 MOVE.B   #$88,D1            SET TRANSFER TYPE TO CYCLE STEAL
                              ****************DMA IN*****************************************************
    00001022 283C5A5A5A5A START       MOVE.L   #$5A5A5A5A,D4      FIRST DATA PATTERN RECIEVED
    00001028 6122                     BSR.S    DMAIN

    0000102A 283CA5A5A5A5             MOVE.L   #$A5A5A5A5,D4      SECOND DATA PATTERN RECIEVED
    00001030 611A                     BSR.S    DMAIN

    00001032 7800                     MOVE.L   #$00000000,D4      THIRD DATA PATTERN RECIEVED
    00001034 6116                     BSR.S    DMAIN

    00001036 78FF                     MOVE.L   #$FFFFFFFF,D4      FORTH DATA PATTERN RECIEVED
    00001038 6112                     BSR.S    DMAIN

    0000103A 0C06000B                 CMP.B    #8,D6              CHECK THE NUMBER OF BLOCKS RECIEVED
    0000103E 6708                     BEQ.S    DOUT
    00001040 123C0020                 MOVE.B   #$20,D1            SET TRANSFER TYPE TO BURST MODE
    00001044 4EF81022                 JMP.S    START
    00001048 4EF81104        DOUT     JMP.S    START1



    0000104C 163C0000        DMAIN    MOVE.B   #0,D3
    00001050 46FC2700                 MOVE.W   #$2700,SR          MASK INTERRUPTS
    00001054 33FC04000BFF             MOVE.W   #$400,$FFE00A      LOAD TRANSFER COUNT
             E00A
    0000105C 23FC00041000             MOVE.L   #$41000,$FFE00C    LOAD MEM ADD COUNT
             00FFE00C
    00001066 13FC000000FF             MOVE.B   #$00,$FFE000       CLEAR CSR
             E000
    0000106E 13C100FFE004             MOVE.B   D1,$FFE004         SET TRANSFER TYPE
    00001074 13FC00B200FF             MOVE.B   #$B2,$FFE005       LOAD DCR
             E005
```

```
0000107C 13FC004400FF         MOVE.B   #$44,$FFE04D        LOAD ATTN INT VECTOR
         E04D
00001084 13FC004000FF         MOVE.B   #$40,$FFE025        LOAD DMA INT VECTOR
         E025
0000108C 21FC000010C8         MOVE.L   #ATTN1,$110         ATTN VECTOR LOCATION
         0110
00001094 21FC0000122C         MOVE.L   #I13,$104           DMA ERROR
         0104
0000109C 21FC000010E2         MOVE.L   #DONE1,$100         DMA DONE VECTOR
         0100
000010A4 13FC003900FF         MOVE.B   #$39,$FFE065        LOAD LWORD* ADDR MODIFIER
         E065
000010AC 13FC001D00FF         MOVE.B   #$1D,$FFE045        ATTN CONTROL REG,LEVEL 5 INT.
         E045
000010B4 13FC001000FF         MOVE.B   #$10,$FFE061        SPARE, ATTN ENABLE
         E061
000010BC 46FC2000             MOVE.W   #$2000,SR
000010C0 0C030001    SELF2    CMP.B    #1,D3               WAIT FOR INTERRUPT
000010C4 66FA                 BNE.S    SELF2
000010C6 4E75                 RTS
                     ****************ATTN1 INTERRUPT SERVICE ROUTINE**********************************
000010C8 13FC003D00FF ATTN1   MOVE.B   #$3D,$FFE047        ENABLE DMA INT
         E047
000010D0 13FC008800FF         MOVE.B   #$80,$FFE007        START DMA CONTROLER
         E007
000010D8 13FC000300FF         MOVE.B   #$03,$FFE061        ENABLE ATTN INT OUT, BO BIT SET, RECEIVE
         E061
000010E0 4E73                 RTE

                     ************************************************************************************
                     ****************DONE1 DMA INTERRUPT SERVICE ROUTINE*********************************
                     *****THIS ROUTINE CHECKS THE RECIEVER BUFFER FOR DATA ERRORS*************************
                     ************************************************************************************

000010E2 5206        DONE1    ADD.B    #1,D6
000010E4 163C0001             MOVE.B   #1,D3
000010E8 287C00041000         MOVE.L   #$41000,A4          BEGINNING ADDRESS OF DATA BLOCK
000010EE 303C0000             MOVE.W   #0,D0
000010F2 2A1C        NOSHIFT  MOVE.L   (A4)+,D5            CHECK DATA
000010F4 BA84                 CMP.L    D4,D5
000010F6 66000154             BNE.L    DATAERR
000010FA 5240                 ADD.W    #1,D0
000010FC 0C400400             CMP.W    #$400,D0
00001100 66F0                 BNE.S    NOSHIFT
00001102 4E73                 RTE

                     **************DMA OUT**********************************************************
00001104 163C0000    START1   MOVE.B   #0,D3
00001108 1C3C0000             MOVE.B   #0,D6
0000110C 123C00B8             MOVE.B   #$B8,D1             SET TRANSFER TYPE TO CYCLE STEAL
00001110 13FC008000FF         MOVE.B   #$80,$FFE063
         E063

00001118 283C5A5A5A5A START2  MOVE.L   #$5A5A5A5A,D4       FIRST DATA BLOCK TRANSFERED
0000111E 612A                 BSR.S    LDMEM1
00001120 613A                 BSR.S    DMAOUT

00001122 283CA5A5A5A5         MOVE.L   #$A5A5A5A5,D4       SECOND DATA BLOCK TRANSFERD
```

```
00001128 6120                     BSR.S     LDMEM1
0000112A 6130                     BSR.S     DMAOUT

0000112C 7800                     MOVE.L    #$00000000,D4        THIRD DATA BLOCK TRANSFERED
0000112E 611A                     BSR.S     LDMEM1
00001130 612A                     BSR.S     DMAOUT

00001132 78FF                     MOVE.L    #$FFFFFFFF,D4        FORTH DATA BLOCK TRANSFERED
00001134 6114                     BSR.S     LDMEM1
00001136 6124                     BSR.S     DMAOUT

00001138 0C060008                 CMP.B     #8,D6                CHECK NUMBER OF BLOCKS TRANSFERED
0000113C 6708                     BEQ.S     DIN
0000113E 123C0028                 MOVE.B    #$28,D1              SET TRANSFER TYPE TO BURST MODE
00001142 4EF81118                 JMP.S     START2
00001146 4EF81010        DIN      JMP.S     RESTART

0000114A 41F900040000 LDMEM1      LEA       $40000,A0            LOAD DATA BLOCK
00001150 20C4            INITMEM1 MOVE.L    D4,(A0)+
00001152 B1FC00041000             CMPA.L    #$41000,A0
00001158 66F6                     BNE.S     INITMEM1
0000115A 4E75                     RTS

0000115C 46FC2700        DMAOUT   MOVE.W    #$2700,SR            MASK INTERUPTS
00001160 163C0000                 MOVE.B    #0,D3
00001164 13FC004500FF             MOVE.B    #$45,$FFE04D         LOAD ATTN. INTERRUPT VECTOR
         E04D
0000116C 13FC004600FF             MOVE.B    #$46,$FFE025         LOAD DMA INTERRUPT VECTOR
         E025
00001174 13FC000B00FF             MOVE.B    #$B,$FFE007          ENABLE DMA INTERRUPTS
         E007
0000117C 13C100FFE004             MOVE.B    D1,$FFE004           SET UP TRANSFER TYPE
00001182 13FC000000FF             MOVE.B    #$00,$FFE000         CLEAR CSR
         E000
0000118A 13FC003900FF             MOVE.B    #$39,$FFE065         LOAD LWORD# AND ADDRESS MODIFIER
         E065
                         ********************************************************************************
                         ************68000 TYPE CPU'S MULTIPLY THE INTERRUPT VECTOR BY 4*****************
                         ***********DURING AN INTERRUPT CYCLE.  EXAMPLE :  $45 *$4 = $114****************
                         ********************************************************************************

00001192 21FC000011FA             MOVE.L    #ATTN,$114           ATTN INT VECTOR LOCATION
         0114
0000119A 21FC0000121C             MOVE.L    #DONE,$118           DMA DONE VECTOR LOCATION
         0118
000011A2 21FC0000122C             MOVE.L    #113,$11C            DMA ERROR VECTOR TO LOCATION 113
         011C
                         ********************************************************************************


000011AA 33FC040000FF             MOVE.W    #$400,$FFE00A        LOAD TRANSFER COUNT
         E00A
000011B2 23FC00040000             MOVE.L    #$40000,$FFE00C      LOAD MEM ADD COUNTER
         00FFE00C
000011BC 13FC003200FF             MOVE.B    #$32,$FFE005         LOAD OCR
         E005
000011C4 13FC001E00FF             MOVE.B    #$1E,$FFE045         ATTN CONTROL REG. LEVEL 6 INT.
         E045
```

```
000011CC 13FC000800FF          MOVE.B  #$08,$FFE061          SET FNCT3 BIT TO DR11W2 BOARD
         E061
000011D4 267C00FFE060 WAIT     MOVE.L  #$FFE060,A3
000011DA 3013                  MOVE.W  (A3),D4               WAIT FOR DR11W2 TO RESPOND
000011DC 02440080              AND.W   #$0080,D4             WITH FNCT3 BIT SET
000011E0 0C440080              CMP.W   #$0080,D4
000011E4 66EE                  BNE.S   WAIT
000011E6 13FC001200FF          MOVE.B  #$12,$FFE061          ENABLE ATTN OUT,ATTN IN
         E061
000011EE 46FC2000              MOVE.W  #$2000,SR
000011F2 0C030001     SELF1    CMP.B   #1,D3                 WAIT FOR SOMETHING TO HAPPEN
000011F6 66FA                  BNE.S   SELF1
000011F8 4E75                  RTS



                      ************ATTN INTERRUPT SETVICE ROUTINE**************************************

000011FA 13FC008000FF ATTN     MOVE.B  #$80,$FFE063          ATTN SERVICE ROUTINE.
         E063
00001202 13FC003D00FF          MOVE.B  #$3D,$FFE047          LOAD DICR (ENA DMA INTERRUPT)
         E047
0000120A 13FC008800FF          MOVE.B  #$88,$FFE007          START DMA CONTROLER
         E007
00001212 13FC000500FF          MOVE.B  #$05,$FFE061          HIT GO BIT TO ENABLE HANDSHAKE
         E061
0000121A 4E73                  RTE



                      *****DMA DONE INTERRUPT SERVICE ROUTINE****************************************

0000121C 5206         DONE     ADD.B   #1,D6
0000121E 163C0001              MOVE.B  #1,D3
00001222 13FC000000FF          MOVE.B  #$00,$FFE063          TURN LED OFF
         E063
0000122A 4E73                  RTE


0000122C 4BF81237     113      LEA     MS63,A5               DMA ERROR ROUTINE
00001230 4DF81248              LEA     ENMS63,A6
00001234 4E4F                  TRAP    #15
00001236 00                    DC.B    0

00001237 0D0A         MS63     DC.B    $D,$A
00001239 4D4153544552          DC.B    'MASTER DMA ERROR'
00001249 0D0A                  DC.B    $D,$A
0000124B              ENMS63


0000124C 4BF8125C     DATAERR  LEA.L   DERR,A5
00001250 4DF8126C              LEA.L   ENDERR,A6
00001254 4E4F                  TRAP    #15
00001256 0006                  DC.W    6
00001258 4E4F                  TRAP    #15
0000125A 0000                  DC.W    0

0000125C 0D0A         DERR     DC.B    $D,$A
```

```
0000125E 444154412045              DC.B    'DATA ERROR'
00001268 0D0A                      DC.B    $D,$A
0000126A 0D0A                      DC.B    $D,$A
0000126C                  ENDERR

0000126C 0D0A             MS68     DC.B    $D,$A
0000126E 444D41205445              DC.B    'DMA TEST IS IN PROGRESS'
00001285 0D0A                      DC.B    $D,$A
00001287 464C41534849              DC.B    'FLASHING LEDS INDICATE A PASSING TEST'
000012AC 0D0A                      DC.B    $D,$A
000012AE                  ENMSS8

                                   END

****** TOTAL ERRORS      0--
****** TOTAL WARNINGS    0--
```

SYMBOL TABLE LISTING

SYMBOL NAME	SECT	VALUE	SYMBOL NAME	SECT	VALUE
ATTN		000011FA	I13		0000122C
ATTN1		000010C8	INITMEM1		00001150
DATAERR		0000124C	LDMEM1		0000114A
DERR		0000125C	MS63		00001237
DIN		00001146	MS68		0000126C
DMAIN		0000104C	NOSHIFT		000010F2
DMAOUT		0000115C	RESTART		00001010
DONE		0000121C	SELF1		000011F2
DONE1		000010E2	SELF2		000010C0
DOUT		00001048	START		00001022
ENDERR		0000126C	START1		00001104
ENMS63		00001248	START2		0000111B
ENMS68		000012AE	WAIT		000011D4

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